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SUPER-HETERODYNE C-PROBE DESIGN AND IMPLEMENTATION

by

Scott A. Heritsch

A thesis submitted in partial fulfillment
of the requirements for the degree

of

MASTER OF SCIENCE

in

Electrical Engineering

Approved:

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1997

ABSTRACT

Super-Heterodyne C-Probe Design and Implementation

by

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Utah State University, 1997

Major Professor: Dr. Charles M. Swenson
Department: Electrical and Computer Engineering

Modern advances in chip design and implementation have provided atmospheric scientists with the tools needed to advance the evolution of atmospheric probes, especially the impedance probe. The impedance probe measures the in-phase and out-of-phase components of the antenna's current with respect to the applied sinusoidal steady-state voltage. Through the integration of super-heterodyne circuitry with previous impedance probe designs, I was able to transfer the in-phase and out-of-phase components of an antenna's impedance in a plasma from 3 MHz to 23.25 KHz. By reducing the frequency of the information signal, it was easier to detect the in-phase and out-of-phase components. The sensitivity of the design was hindered by the inconsistency of the programmable logic chip used to create in-phase and out-of-phase reference signals; however, the overall design concept was proven to work.

(99 pages)

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CHAPTER I

INTRODUCTION

A. Spin-Off Science of the Space Race

At the end of World War II, the United States War Department found itself with a new weapon: the atomic bomb. Successfully demonstrated in both the desert of New Mexico and on the island of Japan as a weapon of deterrence, this awesome force became an even more effective weapon when coupled with the range of a long-range rocket. Towards the end of the war, the Germans had made bounding steps in the development of long-range rockets, which were used to attack London on a limited basis. The secrets and many of the research scientists who developed the most successful of the German rocket experiments, the V2 Rocket, were procured by both the Soviets and the Americans. Each country quickly ran home to experiment with their new assets, creating a highly contested development effort called the space race. Each country tried to outdo the other in developing launch vehicles that carried satellites and astronauts into space, but in a more subtle fashion, they were more concerned with the message of nuclear superiority. Most of the initial research done on the V2s was done in the late 1940s and early 50s. These workhorses provided highly celebrated rocket scientists such as Dr. Werner Von Braun, with the knowledge needed to quickly advance the evolution of the rocket age. However, along with the advances in rocketry came an unexpected advance in atmospheric sciences.

The V2s were equipped with a radio frequency (RF) transmitter that would send telemetry data from the rocket down to the ground stations where the rocket scientists would monitor the flight characteristics, as well as on-board guidance and control. These radio transmitters were transmitting at a frequency between 1 and 3

MHz. When the rockets reached an altitude of about 70 km, the received telemetry signal began to fade, until it was lost altogether. Once the rocket fell below 70 km on its ballistic trajectory, the signal was reacquired. Although the initial intention of these launches was to research the ballistic characteristics of the V2, the incidental loss of telemetry spurred interest in researching the transmission of RF waves through the medium of space [1].

Many years earlier, pioneers in atmospheric science and electromagnetics such as Marconi, Kennelly, and Heaviside postulated that there was a layer that existed in the upper atmosphere where a heavy concentration of ions existed called the ionosphere [2]. Their predictions and postulations were based on observations and measurements made with radio transmitters and receivers in the early part of the century. They found that a radio signal can travel across a greater portion of the Earth's surface than the direct line of sight path it was expected to follow. Actually, at night it could sometimes travel around the world. Their only explanation for this was that there was a reflective layer in the upper atmosphere that had a dielectric constant less than the lower atmosphere. This change in ε allowed for reflections to occur and when a specific angle was exceeded, called the Brewsters Angle, 100% reflection of the propagating wave occurs.

Until the V2 rockets flew to the edge of space and back, there were no recorded man-made objects that had achieved this feat. The loss of the telemetry signal had been the first *in situ* measurement made in the ionosphere. Although the reflection of the radio signals discovered by Marconi and Heaviside and the loss of signal from the V2s are caused by a change in dielectric in the space medium, their effects on the RF systems are different. Marconi's and Heaviside's RF waves were generated on the

ground and then propagated to the ionosphere. The V2's RF waves were created in the ionosphere and never reached the ground. The reason for this was that the transmitters used on the V2 were matched to their transmitting antennas to maximize the power output of the system on the ground. When the rocket was at an altitude of 600 km, the transmitting antenna was immersed in the ionosphere, the dielectric of the medium changed the fundamental characteristics, or impedance, of the antenna, and the power that the transmitter put out at 1 to 3 MHz significantly decreased to the point where the ground stations were unable to pick up the signal. This was the first observation of an effect which would eventually be used to probe the nature of the ionosphere. This thesis details the latest generation of instrument built to measure the ionosphere based on the changing impedance of an antenna immersed in the earth's ionosphere.

B. Nature of the Ionosphere

Kennelly and Heaviside defined the ionosphere as a region of the atmosphere consisting of ions, which stretches from about 70 km above the earth to 1000 km [2]. Our understanding of the ionosphere has vastly improved since the 1950s to the point where computer models have been developed. The ionosphere is composed of both neutral and ionized gasses called plasma. The amount of plasma produced depends on the density of neutral gasses and the amount of high-energy ultraviolet radiation the ionosphere is exposed to. This radiation provides enough energy when absorbed by a neutral gas atom or molecule that an electron is ejected from its shell and becomes a free-floating electron. The remaining one atom or molecule become a positively charged ion. The composition and density of the ionosphere follows a daily cycle based on the position of the sun in the sky. Solar events such as a solar flare can cause the ionosphere's electron density to increase beyond its normal density and provide

scientists with an opportunity to evaluate unique solar/terrestrial interactions. Since the electrons and ions originate from the same neutral atom or molecule, the ionosphere is composed of the same number of electrons as positive ions, and hence the total amount of plasma can be determined by measuring the number of free electrons in a given region of space. This electron density is a fundamental parameter of the ionosphere that governs its effect on EM waves. Figure 1 [3] illustrates typical electron densities found in the ionosphere based on altitude and time of day as well as the changes that occur on an 11-year solar cycle. As the trace in Figure 1 migrates to the right, the ionosphere is said to be hardening. This refers to an increase in electron density.

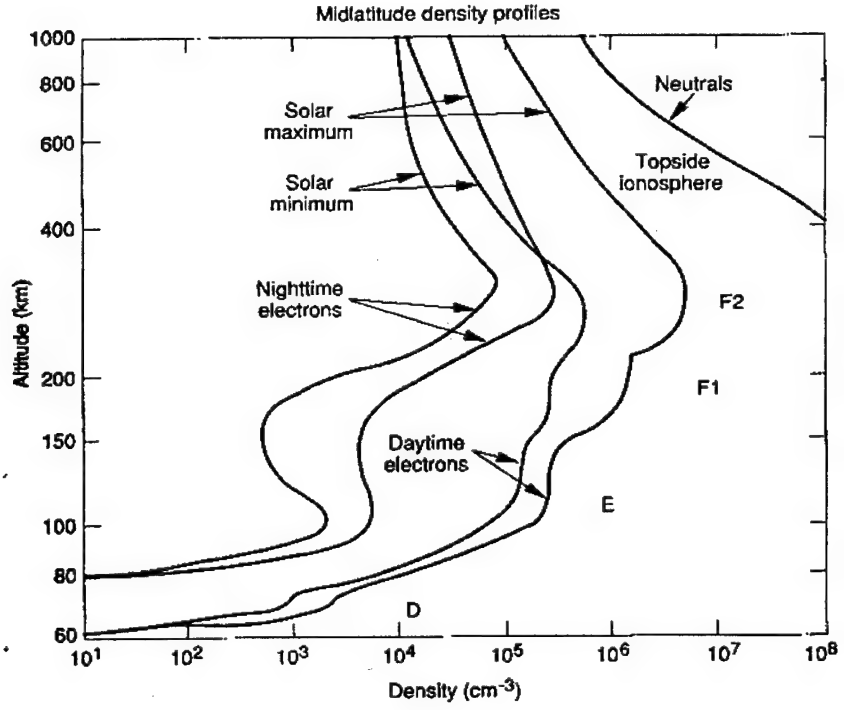

Fig. 1. Electron densities in the ionosphere.

C. Measuring Electron Density In Situ

The ionosphere is broken into regions as described in the above figure. These regions are characterized by the electron density in the region as well as the existence of specific species of atoms. Different species absorb different wavelengths of radiation and cause the ion electron density in that particular region to be based mostly on that particular species giving up a free electron. The ionosphere is responsible for effects such as scintillation on radio transmissions to and from spacecraft, transionosphereic currents in high-latitude power grids, location errors in Global Positioning System (GPS) signals, RF transmission beyond line of sight, and short wave radio fade [4]. As we become more dependent on technology, especially telecommunications, it becomes far more important to understand the effect the ionosphere has on the operation of modern technology. It is hoped that the current research of the ionosphere will provide us with a more accurate method to understand and/or predict these space weather effects.

Before the first sounding rocket ever left the launch pad, most of what we knew about the ionosphere was through ionosondes. These devices reflected electromagnetic (EM) waves of various frequencies off the ionosphere. Different frequencies are partially reflected at altitudes correlating to different electron densities. The classification for ionospheric regions shown in Figure 1 originated from this probing technique.

One might argue that the first *in situ* measurements of the ionosphere were made using the radio beacons on early V2 rockets as previously described. Although the RF attenuation experienced during these initial V2 launches was not intentional, it did spark interest in flying a series of ionospheric probes [1]. At the time the only *in*

situ instrument available for dedicated ionospheric study was the Langmuire probe. This probe was originally developed to measure the plasma density in a laboratory environment [2]. The sounding rocket launches made into the ionosphere provided scientists with the first opportunity to measure a natural plasma outside of the laboratory. The Langmuire probe measures the number of electrons collected by a charged plate or antenna in the form of direct current (DC). This is why the Langmuire probe is often called a DC probe. The DC probe was very useful in providing much of the data now used to characterize the ionosphere. At first, these probes were included as secondary payloads opposite the ballistic tests. As the interest in upper atmospheric research grew, these plasma probes began to warrant their own rockets and soon a series of sounding rockets dedicated to the scientific exploration of the upper atmosphere began to launch out of Wallops Island VA and White Sands NM in the late 40s and early 50s.

The next generation of probes developed specifically to measure the electron content of the ionospheric were the impedance probes. This technique used an RF signal to measure the impedance of an antenna immersed in the ionospheric plasma. The impedance or RF probe has become a whole family of probes, often called capacitance, Z, theta, or plasma frequency probes. These probes generally provide more accurate measurements of electron density than the Langmuire or DC probe, which give relative density. The impedance probes use both the imaginary and real components of the impedance of an antenna immersed in a plasma to derive the electron density. This is done using the following equation.

$$n_e = \frac{\omega^2 m_e \varepsilon_o}{e^2} \frac{\Delta X + \frac{(\Delta R)^2}{\Delta X}}{\Delta X + \frac{(\Delta R)^2}{\Delta X} + X_o} \frac{C_{sh} + C_o}{C_o} \qquad \textbf{(1-1)}$$

where:

ω = Probe excitation angular frequency (rad/sec)
ΔX = Change in series antenna reactance in a plasma from its free space value
ΔR = Change in series antenna resistance in a plasma from its free space value
$X_o = 1/(\omega C_o)$ = Free space series reactance of the antenna
C_{sh} = All capacitance shunting the antenna that is not in the plasma

The modern capacitance probe (C-probe) has suffered in accuracy because of both the method of implementation and the accuracy of the individual components. Measuring the in-phase and out-of-phase components at 3 MHz is more susceptible to constant phase errors than measuring at 25 KHz. Recently through the efforts of Dr. Earl Pound, these issues were being addressed with a proposed super-heterodyne capacitance probe design [5]. The present C-probes lack the ability to accurately measure the small real or resistive component of the antenna's impedance. This particular method has the benefit of finding both the small real and larger imaginary, or reactive components of the impedance. These upgrades to the current C-probe design will bring the scientific community closer to accurately measuring the properties of the lower ionosphere where this technique excels above others.

D. Outline of the Rest of the Thesis

The projects goal was to design, build, and test Dr. Earl Pound's super-heterodyne impedance probe that was capable of accurately measuring both the real and imaginary components of an antenna's impedance in ionospheric plasma. The construction must be flight worthy and ready for launch on the COORS rocket out of

the Wallops Flight Facility. Chapter II discusses the science behind the impedance probe and super-heterodyne system. It illustrates why the super-heterodyne technique is ideal for the problem of measuring the real and imaginary components of the antenna impedance. Chapter III goes through the design phase of the Chemistry of Odd Oxygen Rocket with SPAAS (COORS) super-heterodyne C-probe step-by-step and illustrates what the expected outputs for each stage of the system are. It will also talk about some of the unique circuits that are required to make the super-heterodyne system work. Chapter IV is dedicated to the circuit design and layout. It illustrates the integration of the new super-heterodyne design with an older C-probe design used for the Chemistry and Dynamics of Odd Oxygen (CADO) launch, which was the predecessor to COORS, and how both the schematic and trace layout are affected by alterations made from CADO as well as the high frequency specifications required for the new probe. Chapter V shows the steps involved in constructing each section of the impedance probe circuit. Since each circuit subsection is dependent on the output of the preceding circuit sub-section, I provide the output for each section and evaluate its ability to effectively drive the next section in line. In this chapter, I also address the changes that occur when the DC-to-DC converters are added and the circuit is placed in the payload. Chapter VI has the antenna calibration data of the impedance probe. This information is used to assess the performance of the super-heterodyne probe as compared with other probes. Chapter VII presents the conclusion of the thesis, the performance evaluation, and recommendations for further research.

CHAPTER II

THE SCIENCE OF THE SUPER-HETERODYNE IMPEDENCE PROBE

A. *Measuring the In- and Out-of-Phase Components of Impedance*

Physically measuring the impedance of an antenna can first be done by applying a sinusoidal voltage across the antenna. Using the simple Z=I/V relationship, we can determine the impedance by measuring the current produced from the known voltage source. Since the voltage source is a sinusoidal source, we need to measure both the magnitude and phase of the current to fully characterize it. Current can be represented in either polar form as magnitude and phase or in rectangular form as the in-phase component or out-of-phase component. We have chosen to measure current in rectangular form. This is accomplished by mixing the current signal with two reference sinusoids of the same frequency. The first sinusoid is in phase with the voltage signal while the second is 90° out of phase. Previous C-probes have had to perform this mixing process at frequencies close to 3 MHz. With the super-heterodyne technique, the antenna is still driven at around 3 MHz, but the in-phase and out-of-phase detection is done at around 50 kHz. Simply put, the super-heterodyne method places the phase detection circuitry at a lower frequency, therefore making it less susceptible to phase errors, which are independent of frequency. Assuming a constant phase error, lower detection frequencies will have a lower percentage of their phase subject to error than would higher frequencies. Figure 2 illustrates the benefit of reducing the detection frequency.

Both plots have the same phase shift. However, we can see that for a given time delay, the percent error in the higher frequency plot would be much greater and the overall detection of the lower frequency would be easier. This is the basis of the super-heterodyne system where the lower frequency produced by the super-heterodyne system is referred to as the intermediate

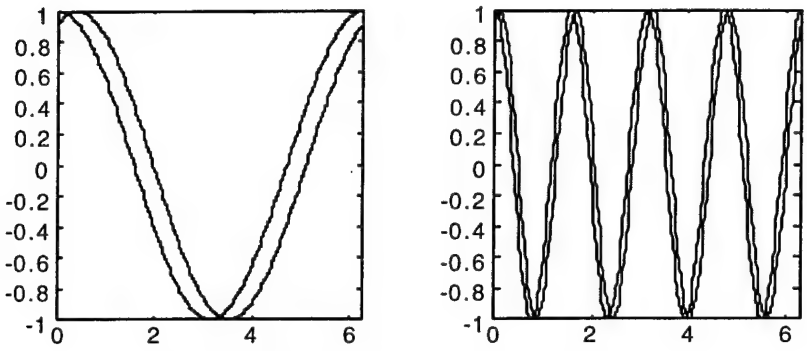

Fig. 2. Differences in phase detection.

frequency. However, in order to get the in-phase and out-of-phase components, we need to compare it with reference signals that are at the intermediate frequency. This requires that the same source used to create the antenna drive signal be independently reduced to the intermediate frequency without any phase delays in the process using high-speed dividers. Figure 3 shows the flow diagram of the super-heterodyne system when implementing a C-probe [6].

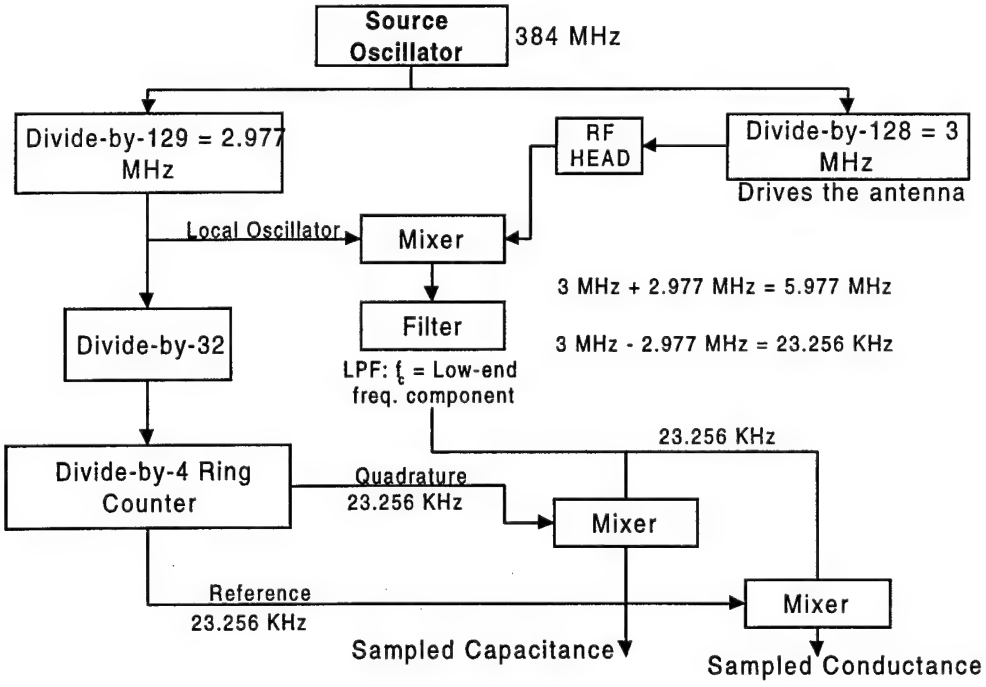

Fig. 3. Super-heterodyne flow diagram.

This diagram will be the basis for the rest of the discussion of the super-heterodyne method. We start with a source frequency that is much higher than our required antenna drive frequency so that we get a local oscillator and an antenna drive signal, which are locked in phase relative to each other. This is needed in order to successfully split the paths, one for the antenna and one for the reference signals. Using concurrent dividers makes the implementation of this super-heterodyne system much simpler than using non-concurrent dividers. Figure 3 uses a division ratio of 128/129 for the purpose of illustrating this point. Table I shows how different division ratios set what source frequencies are needed and what the intermediate frequency will be. The constant variable throughout all this is the required 3-MHz antenna drive frequency. Table I illustrates a tradeoff that must be made between the intermediate frequency and the source frequency. These are inversely related and the pair chosen must be based on the sensitivity of the components being used. Only recently have frequency synthesizers reached a level of speed that would allow for the 128/129 and 256/257 division ratios to be used.

The concurrent division ratio provides a problem with hardware implementation. Simple flip-flops can be used to get a division ratio for any power of 2, but to get a division ratio of $2^N + 1$ requires a more complex method. Luckily, the commercial communications industry has

TABLE I
SUPER-HETERODYNE DIVISION RATIOS FOR 3-MHZ DRIVE FREQUENCY

Concurrent Division Ratios	Source Frequencies (MHz)	Intermediate Frequencies (kHz)
4/5	12	600
8/9	24	333.33
16/17	48	176.47
32/33	96	90.909
64/65	192	46.153
128/129	384	23.255
256/257	768	11.673

provided a solution to this problem by solving a problem of their own. Cellular phones use concurrent division ratios in their phase locked loop (PLL) circuitry. The industry uses division ratios from 4/5 to 128/129 and has made them commercially available as programmable pre-scalers.

B. RF Head Design

After the concurrent division ratios, the flow diagram splits into two sections. The next important step is the antenna section. The antenna and accompanying circuitry are often referred to as the RF Head, which consists of matched current transformers. The current transformers isolate the antenna from the rest of the circuit and allow the current's magnitude and phase information to be generated without affecting the load on the antenna. The parallel pathways provide for a symmetric circuit. This allows us to calibrate out C_o, or free space capacitance of the antenna, which means that all we are measuring is ΔC or relative change in capacitance. This increases the sensitivity of the circuit while at the same time providing us with the value for the free space capacitance of the antenna, C_0.

C. Intermediate Multiplier and Filter

The signal coming out of the RF Head still has a frequency of 3 MHz but contains the phase and amplitude information of the current on the antenna. This is the information that has to eventually be transmitted to the ground. At this point in the flow diagram, the local oscillator signal and the antenna's drive current signal are mixed together. It is easier to evaluate the result of this multiplication in the frequency domain. Figure 4 shows that the output of the multiplication is a combination of sinusoids at sum and difference frequencies with amplitudes related to the original signal amplitudes. Both the frequency components contain the phase and

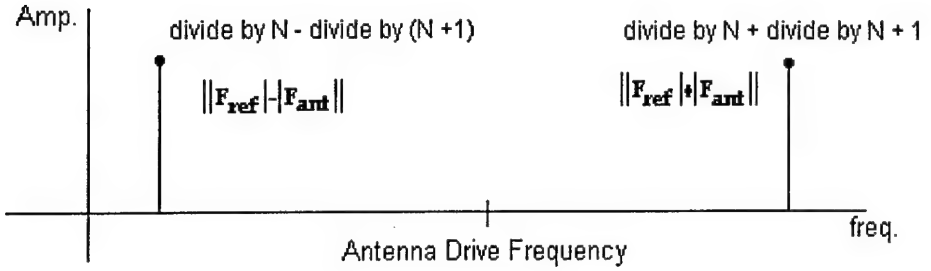

Fig. 4. Theoretical multiplier output.

amplitude information; however, since we want a low intermediate frequency, the higher frequency will be filtered out using a low-pass filter.

D. Reference Signal Division and 4-Ring Counter

So far, only the information or antenna current signal has been discussed. The other half of the super-heterodyne C-probe is the reference signal. This signal is used to determine what phase shifting has been done on the antenna current. In order to accomplish this, successive divisions must be done beyond that of the concurrent divisions to bring the reference down to the intermediate frequency. Fortunately if the lower order primary divider is a power of 2, so will be the required secondary divider. In a super-heterodyne system utilizing concurrent primary dividers, the secondary divider will be equal to the higher order primary divider. The following equations illustrate the point. Equation 2-1 shows what happens when the two concurrent frequencies are multiplied and filtered, while Equation 2-2 shows why the secondary divider is equal to the lower order divider (N) assuming that is the divider used to produce the antenna drive frequency.

The reference signals for measuring the in-phase and out-of-phase components at the intermediate frequency are finally generated in the "4-ring counter." The 4-ring counter has four

$$\frac{F_{osc.}}{N} - \frac{F_{osc.}}{N+1} = F_{osc.}\left(\frac{N+1-N}{N^2+N}\right) = F_{osc.}\left(\frac{1}{N^2+N}\right) \qquad \textbf{(2-1)}$$

$$F_{osc.} \cdot \frac{1}{N} \cdot \frac{1}{N+1} \qquad = F_{osc.}\left(\frac{1}{N^2+N}\right) \qquad \textbf{(2-2)}$$

outputs, each 90° apart from the next. One of the four signals will have the same phase as the antenna drive signal, while the rest will be 90°, 180°, and 270° apart in phase. By multiplying the 0° and 90° reference signals with the antenna current signal, the in-phase and out-of-phase magnitudes are generated at DC along with a sinusoid at twice the intermediate frequency. A second low-pass filter is used to remove the signal at twice the intermediate frequency. The resulting two DC values are the magnitudes at the in-phase component of the current and out-of-phase component of the current or the conductance (G) and susceptance (B) of the antenna. Since the susceptance is proportional to the capacitance, the susceptance channel is also called the capacitance.

CHAPTER III

DESIGN OF THE CIRCUIT

A. Introduction to Design

This chapter presents the preliminary circuits for each subsection of the super-heterodyne C-probe. The previous chapter showed the super-heterodyne math that was involved in both the super-heterodyne technique and the C-probe, as well as basic block diagram of the system. In this chapter, we go more in depth by first breaking down the functional block diagram into subsections, evaluating the expected inputs and outputs, and then designing circuits that will provide us with these desired outputs. Appendix A has the full schematic for all the designs presented in this chapter.

B. Functional Block Diagram

The following block diagrams show the signal paths of the probe from start to finish. Figure 5 shows the entire system and classifies each section of the probe. The figures that follow the block diagram show the desired output for each section. The implementation of the probe is based on effectively producing these desired outputs. The subsections include the source oscillator, the primary dividers, the RF Head, the RF Head post-amp, the intermediate multiplier, the intermediate filter, the secondary divider, the Altera pre-amp, and the phase discriminators.

The High Frequency section shown in Figure 6 consists of the main oscillator and the concurrent dividers. The output of both dividers is AC coupled before propagating to the next section. The output of the lower order divider is used to drive the RF Head while the other divider's output is used as the local oscillator or reference signal for the intermediate multiplier and phase discriminator.

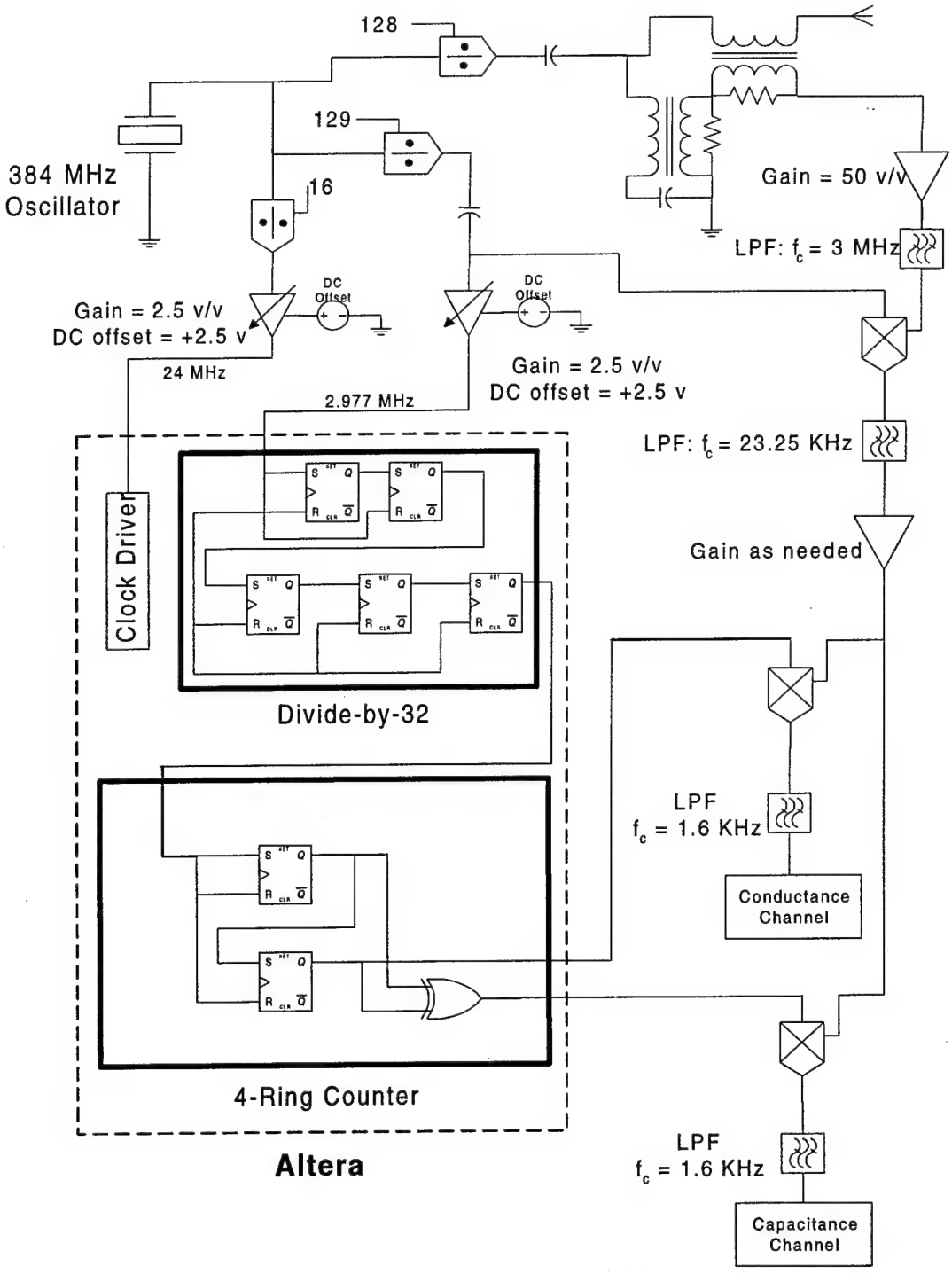

Fig. 5. Full block diagram.

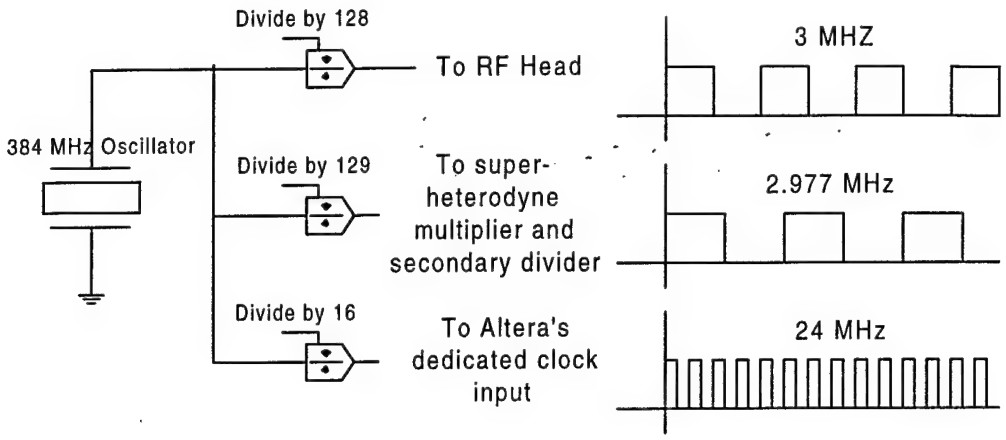

Fig. 6. High frequency block diagram.

The next section is the RF Head and post-amp shown in Figure 7. Here the 3-MHz signal is sent through the RF Head and then conditioned with a post-amp. The post-amp should be able to handle gains up to 50 v/v to amplify the RF Head output to ±1v, and filter out any harmonics, noise, or distortion that results from passing the 3-MHz signal through the RF Head.

The next section is the multiplier and filter stage, which creates the intermediate frequency. This section is depicted in Figure 8. I refer to these two circuits as the intermediate multiplier and intermediate filter, respectively. Any phase information created in the RF Head will also appear at the intermediate frequency. Multiplying the local oscillator/reference signal with the output of the RF Head creates both $(f_1 + f_2)$ and $(f_1 - f_2)$ components, both of which have the phase information contained within them. The filter is used to retrieve the lower frequency components.

In parallel with the intermediate multiplier is the secondary divider. This is used to create a second signal of equal frequency to the intermediate signal and is referred to as the reference signal. The secondary divider consists of two dividers in series. The first divider is a simple n-bit divider. The second divider is a divide-by-4 ring counter. The ring counter divides

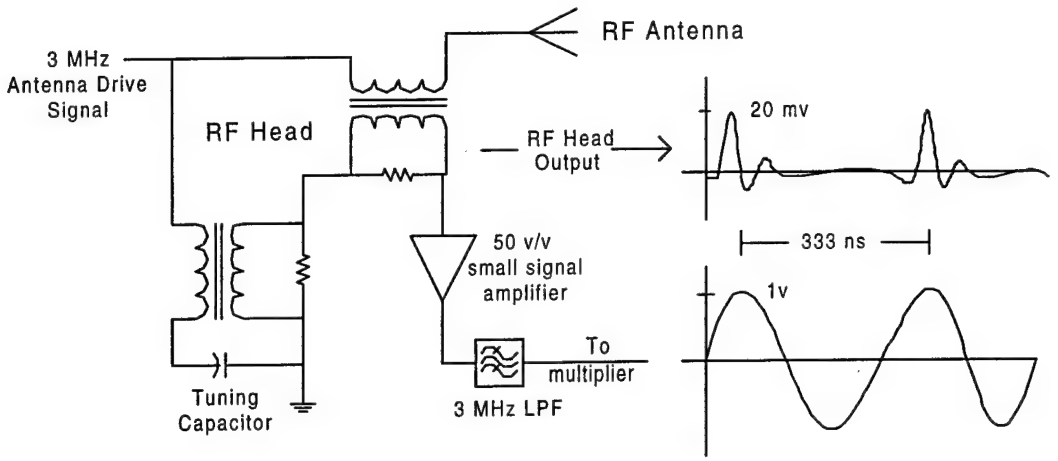

Fig. 7. RF Head and post-amp.

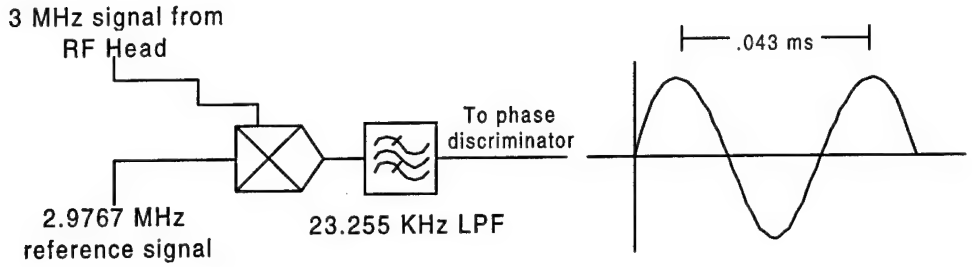

Fig. 8. Intermediate multiplier and filter.

the input by four and then creates four output lines of equal frequency (one fourth of the input frequency) that are 90° out of phase from each other. The reference signal may require conditioning using a pre-amp before entering the secondary divider so that the logic level voltage of the reference signal will be compatible with the logic level voltage required by the logic of the secondary divider. The programmable logic used in implementing the secondary dividers and A/D drivers is an Altera chip. This chip requires a clock input with a frequency of 24 MHz. This is done by dividing the main oscillator and then converting the signal to voltage levels that are ideal with the logic used. Figure 9 illustrates the logic chip configuration while Figure 10 illustrates the logic level converter. The final section is the phase discriminator section. This

consists of a multiplier and filter for each of the conductance and capacitance channels. Since the two signals are of equal frequency and differ only in phase, the low-pass filter will output a DC value that is a function of the difference in phase. Figure 11 shows how this is done. The rest of the circuit is for conditioning the signal for telemetry. This includes A/D and

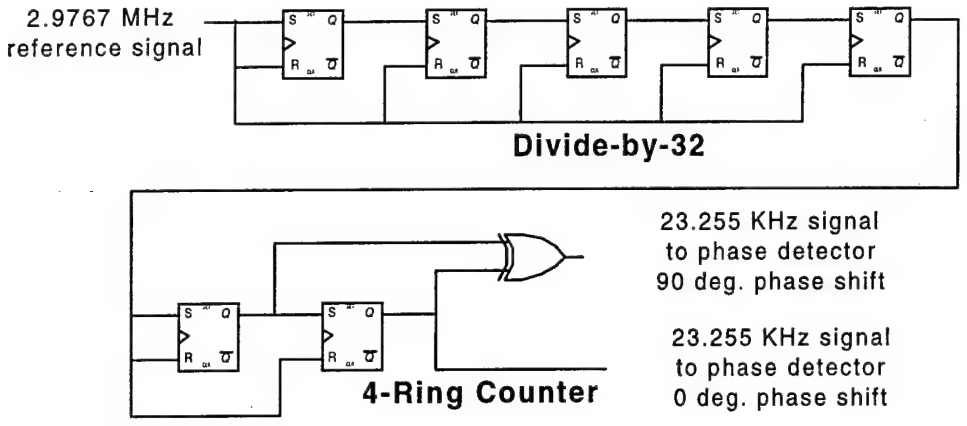

Fig. 9. Secondary divider.

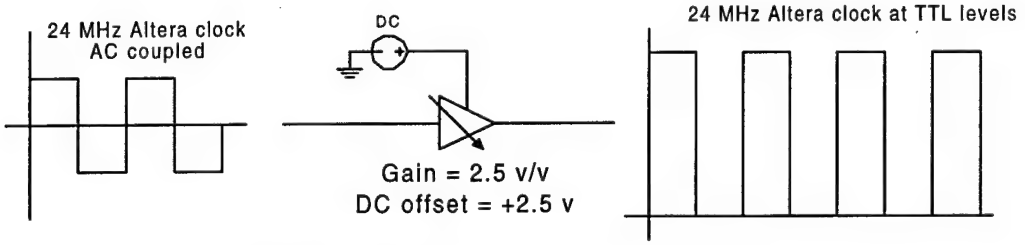

Fig. 10. Clock driver and conditioning amp.

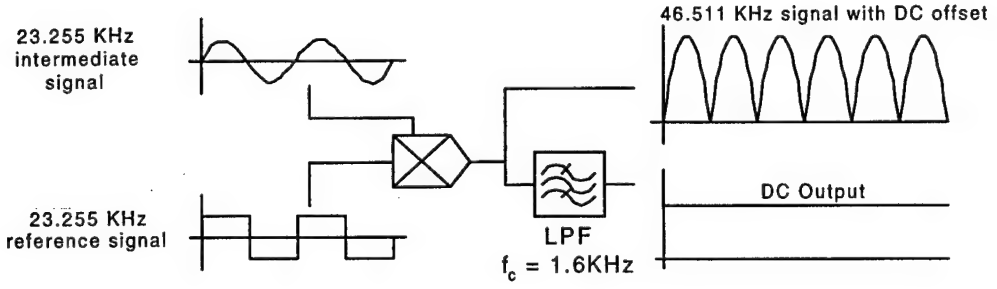

Fig. 11. Phase discriminator.

multiplexing. These features are dependent on the telemetry capabilities of the particular launch vehicle.

C. Dividers

There are two criteria for choosing the appropriate dividers for the super-heterodyne system: the desired intermediate frequency and availability of high-frequency parts to perform this function. The higher order the dividers are, the lower the intermediate frequency will be. However, the higher order the dividers, the higher frequency the primary oscillator must be to create a 3-MHz signal to drive the RF Head. The current ability to implement a low intermediate frequency, super-heterodyne, plasma-impedance probe is based on the recent availability of high frequency dividers with high order division values.

The current accessibility of concurrent, high-frequency dividers has been fueled by the demand for cellular telephones, which use these dividers as prescalers. These prescalers operate at frequencies up to 2.2 GHz if needed, and have their division ratios set by logic inputs. The standard division values for these dividers are usually divided by 2N and 2N+1, which actually are desirable for a super-heterodyne system since the secondary divider has to match the primary divider. These features make the prescalers highly desirable for implementation in a super-heterodyne system. The chips can be purchased from most cellular telephone manufacturers or their suppliers.

In researching the different prescalers available, I have found that their specifications and performance ratings are all very similar and that only a few ratios are really practical. I attribute this to the mass standardization of cellular phone technology in order to meet the current demand as quickly as possible. For our purposes, almost all prescalers meeting the requirements of division ratio and frequency were acceptable. I chose to use the Motorola MC12053A "1.1 GHz Low Power Dual Modulus Prescaler With Stand-By Mode." This model has two division

ratios available, divide by 128/129 and divide by 64/65. This means that if needed, I can change my division ratio by rewiring two logic inputs. Also, because of Motorola's mass production scale, I was able to obtain the chips through samples. These high-speed chips are ECL (emitter coupled logic), which is the only high speed family available. ECL's output voltage offset is related to the chips power voltages, but the peak-to-peak output level is always ≈1 volt. This means that all the ECL chips used must have similar power levels if they are to be compatible with each other. Choosing the correct set of dividers is very important because they will dictate the programmed division value for the secondary divider.

D. Oscillators

The super-heterodyne system requires an oscillator that is significantly higher in frequency than the actual operating frequency of the RF Head. The oscillator's frequency depends on the division ratio chosen for the two dividers. The higher the division ratio is, the greater the initial frequency must be to keep the RF drive frequency at 3 MHz. Assuming that the two dividers are concurrent in value (i.e. ÷128 and ÷129), the initial clock frequency is found by:

RF Drive Frequency * Lower Division Ratio = Oscillator Frequency

What this says is that before an oscillator can be chosen, the initial division ratio must be chosen. For the initial super-heterodyne system, I chose a divide by 128/129 because of availability and the calculated intermediate frequency of 23.26 KHz. This meant that I needed a 384 MHz oscillator to drive the system.

Finding the appropriate oscillator depends on many factors such as device complexity, size, power, cost, compatibility, and precision/stability. I found there to be three main competitors for the super-heterodyne oscillator: the crystal oscillator, the voltage controlled

oscillator, and the phase locked loop. Each of these devices has been widely used and tested in industry so an educated decision can be made without having to test each device. Table II shows how each of the devices compares in the issues stated above. For the COORS payload, space or power did not pose any serious restrictions. This meant that of all the options, the crystal oscillator provided the most stable source oscillator.

Finding a crystal oscillator manufacturer that would make a 384-MHz Oscillator was difficult. The decision to go with Connor Winfield was made because they were the only company researched that could provide an oscillator at 384 MHz with ECL. Adding to the difficulty was the unique frequency of 384 MHz. I found a few places with pre-made oscillators at either 350 or 400 MHz, but all 384 MHz oscillators had to be built from scratch.

TABLE II
TRADE-OFFS FOR PRIMARY OSCILLATOR

Device	Complexity	Size	Power	Cost	Compatibility	Precision/ Stability
Crystal Oscillator	Very Simple Comes ready to use	Large	Medium to heavy usage	depends on precision	Can buy it for TTL, ECL, etc.	Can get up to 5% error in frequency deviation
Voltage Controlled Oscillator	Tank Circuit can be complex	Tank is usually large	Low	Chip is cheap Tank circuit is $$	VCO output is compatible to most logic	Tank is temp. sensitive
Phase Locked Loop	The most complex of the three	Multiple chips in system	Medium usage	Same as VCO	Compatibility based on VCO output	Feedback makes it precise

E. RF Head

The RF Head is a current transformer that isolates the antenna from the rest of the circuit and allows the phase and magnitude information to be passed along to the rest of the circuit. This particular configuration can be modeled by Figure 12, which is the design used by CADO's C-probe.

The defining feature of the RF Head is its symmetry. Under initial operating conditions, the RF Head has two identical pathways for the current to flow. This occurs when the free-space capacitance matches the tuning capacitor, resulting in identical impedances. As the measured capacitance changes, the impedance of that pathway changes, creating a phase and magnitude difference between the two signals. The amount of phase change is directly related to the change in capacitance. It is this change in capacitance that is related to the electron density through Equation 1-1.

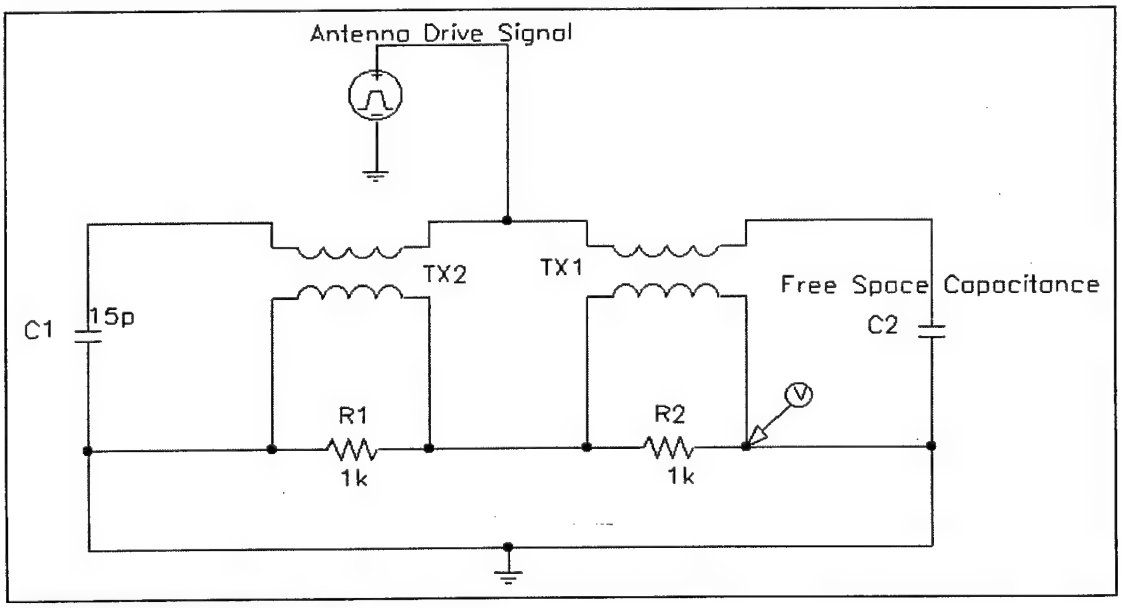

Fig. 12. RF Head model.

The proper operation of the RF Head requires that the tuning capacitor be accurately set to the free-space capacitance of the antenna. In the absence of plasma, both channels are in phase. Unfortunately, for prelaunch testing and calibration, the free-space capacitance of an antenna is very sensitive to its surrounding environment. The free-space capacitance on a laboratory bench can be very different from the free-space capacitance of the antenna at 30-km altitude. In order to effectively tune the RF Head, the probe antenna must be as close to operating conditions as possible when tuning the tuning capacitor [6]. Often this means suspending the probe off the ground and away from any strong electromagnetic fields.

F. RF Head Post-Amp

Following the RF Head is the post-amp. This post-amp must do two separate functions. First, it must amplify the output of the RF Head. The input into the RF Head is actually a square wave instead of a sinusoid. According to previous launches of the RF Head, the predicted output of the RF Head with a square wave input is depicted in Figure 13 [6]. The spikes have a period equal to the RF drive frequency, which means that the fundamental frequency is still present and contains the phase information needed to determine electron density. However, the amplitude of the signal is close to 20 mv, indicating a rather poor frequency response at 3 Mhz. This does not provide a lot of signal power and will probably be lost in the noise by the end of the super-heterodyne circuit. Therefore, an amplifier is used to boost the signal to a high enough level

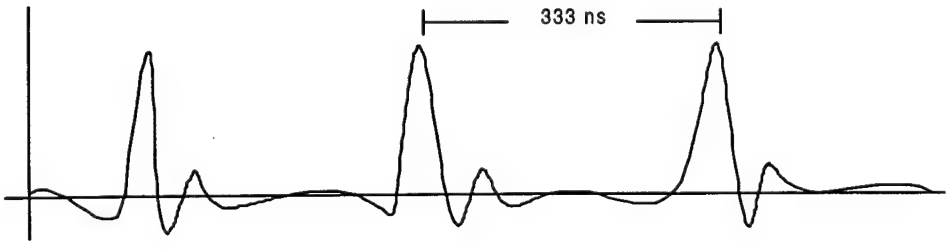

Fig. 13. Predicted output of RF Head.

where the intermediate multiplier can distinguish the input signal from noise. The maximum gain of the amplifier is dictated by the maximum allowable input voltage of the intermediate multiplier. In most cases, this value is 1 volt. This means that the amplifier must have a gain of at least 50 v/v at a frequency of 3 MHz. Because of the high frequency and gain requirements, our selection of suitable amplifiers decreases.

A secondary function that can be done by the post-amp (if desired) is to filter the current signal. Filtering the current signal will isolate the fundamental frequency. This task is not mandatory because the intermediate filter will filter the mixed local oscillator and current signal again after the multiplication. Filtering the RF Head output can be done naturally using the Mean Gain Bandwidth of the op-amp, using an active filter, or even using a passive filter. However, the active and passive filter will introduce a lot more phase shift into the signal and make it more difficult to determine how much of that phase shift is actually caused by the change in capacitance as measured by the antenna.

I chose to keep the post-amp simple and utilize the natural bandwidth of the op-amp to provide limited filtering. I used the following configuration shown in Figure 14 for a simple noninverting amplifier with a gain of 50.

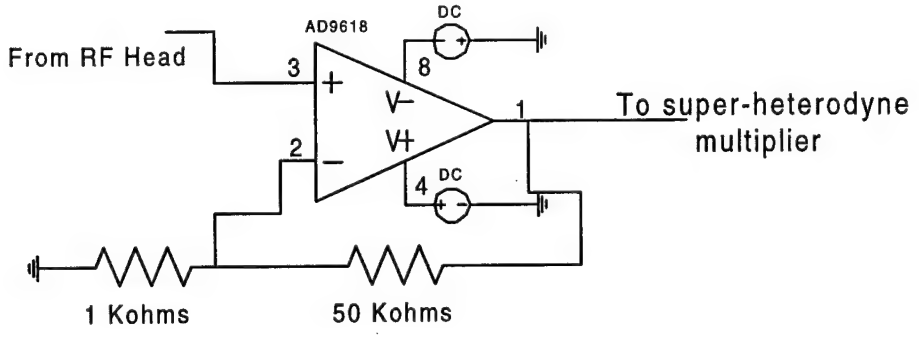

Fig. 14. RF Head post-amp design.

G. Intermediate Multiplier

The task of the intermediate multiplier is to mix the 3-MHz antenna drive signal with the 2.9767 MHz secondary signal to create a lower frequency signal for phase detection. The multiplication creates a waveform consisting of a 5.9767-MHz component and a 23.256-KHz component. Both components contain the phase information introduced by the RF Head. This is the fundamental difference between the super-heterodyne C-probe design and the previous designs. Because of this multiplication procedure, we can run a 23-KHz signal through a phase discriminator instead of the 3-MHz drive frequency, which has been the standard in the past. Making the phase measurements at a lower frequency should improve the accuracy of the measurement.

The criteria for choosing a multiplier are speed and linearity. The multiplier must be able to handle the 3-MHz input. Also, there must be minimal additional phase shift introduced by the multiplier. Previous designs of the C-probe have used the Analog Devices AD834 differential multiplier. However, this design requires a differential op-amp as a follow-on to convert the differential output back into a single ended output. The AD835, which is the successor to the AD834, is a 4-quadrant, single-ended output multiplier. It is capable of frequencies up to 250 MHz and is linear for the full range. The only additional components needed are two resistors to a constant multiplication factor. Figure 15 illustrates the configuration used.

H. Intermediate Filter

The intermediate filter follows the intermediate multiplier and is designed to filter out the 5.9767-MHz component, leaving the 23.256-KHz signal. Ideally there should be only two components to the signal. The filter can be a band-reject filter set for 5.9767 MHz. However, since this filter is the last step before the phase discriminator, and the local oscillator is a square

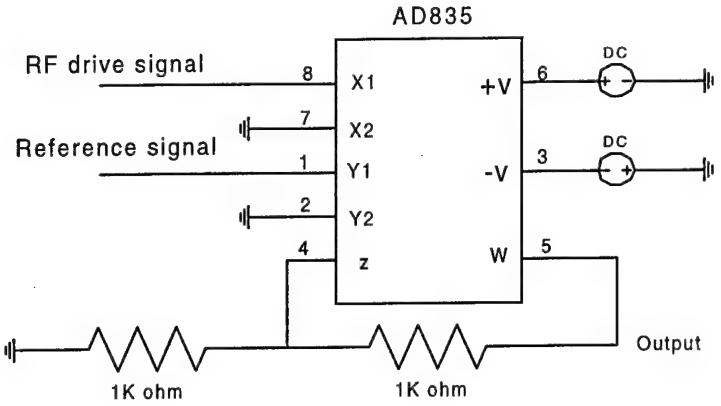

Fig. 15. Intermediate multiplier.

wave, it would be advisable to use a low-pass filter to reject both the 5.9767-MHz component, the harmonics of the square wave, and the high frequency noise that has been introduced along the signal path. This is done using two filters. First, a passive twin-T notch filter is used to sharply cut off the upper frequency and then a simple low-pass filter is used to clean up whatever is left. The benefit of this design is that the cut off frequency of the low-pass filter can be much higher than the lower intermediate frequency and the phase shift induced at the intermediate frequency is much smaller than it would be if the low-pass had a sharper cutoff. Figure 16 shows this in the frequency domain. The filter should be an active filter as opposed to a passive filter to allow for easy implementation of a sharp cutoff. A filter that combines the low-pass and band-reject functions would be ideal but would be costly in terms of circuit board real-estate. This

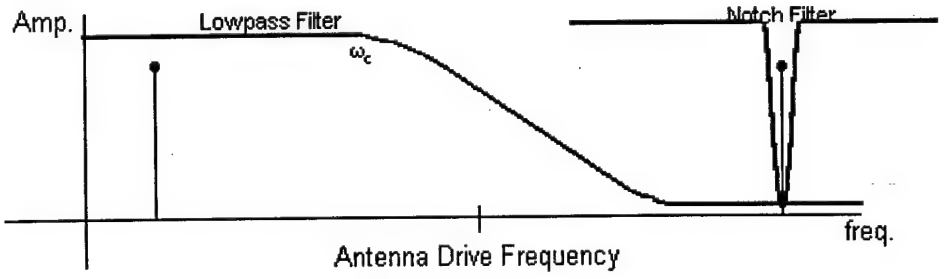

Fig. 16. Intermediate filter.

same response can be achieved with a band-pass filter centered on 23.256 KHz. Figure 17 shows a band-pass filter in an active configuration. The transfer function for this filter is shown in Figure 18.

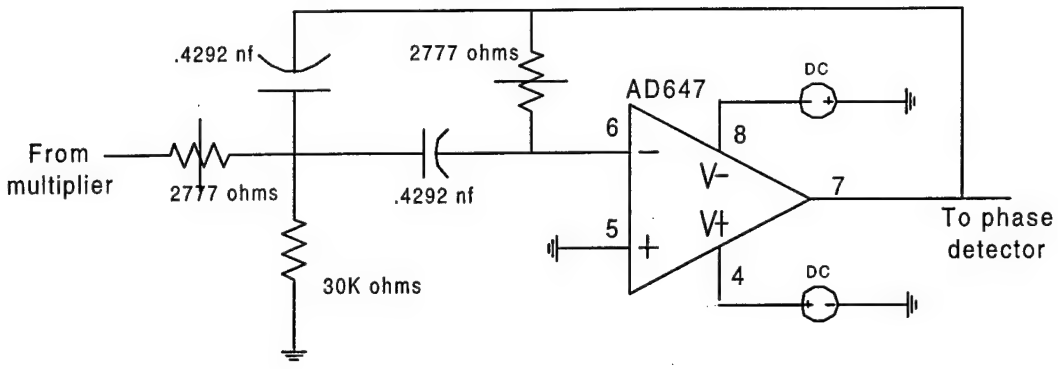

Fig. 17. Intermediate filter circuit.

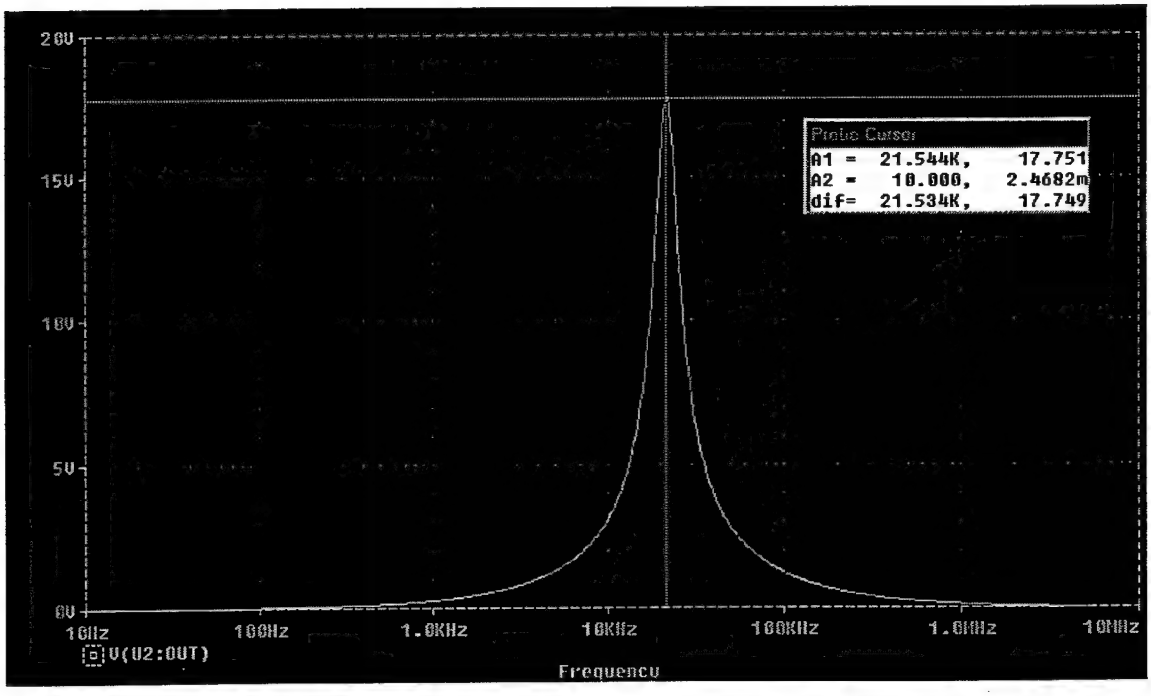

Fig. 18. Band-pass filter transfer function curve.

The greatest concern with the band-pass filter is the phase shift. At the frequency for which the filter is designed there is no phase shift; however, the adjacent frequency on either side has a phase shift of ± 90°. This is caused by a large Q value, which provides a sharp cutoff in magnitude but a steep phase/frequency slope. Unless the filter is perfectly tuned to the exact frequency, there will be a significant phase shift induced. This problem can be resolved either by choosing another filter with a lower Q value ensuring the filter is precisely tuned and the source oscillator is stable, or by pulling off an alternate phase line from the 4-ring counter. Once the circuit is built, the relative phase of the intermediate signal will be known and the necessary phases from the 4-ring counter can be chosen. The phase shift stays at ± 90° on either side of the center frequency for about ± 150 Hz. Choosing the phases after the circuit is built is far more realistic for circuit implementation. By tuning the filter to within 150 Hz of the center frequency, the phase shift can be measured and summarily used in planning the appropriate output phase of the 4-ring counter.

I. Secondary Dividers

The purpose of the secondary divider is to reduce the frequency of the reference signal to equal to the intermediate frequency of 23.256 KHz. Since we are using a divide by 128/129, the secondary divider must be a divide by 128. (The secondary divider is always equal to the lower of the two concurrent dividers.) In order to keep the secondary divider simple, it is advisable to keep its division value at a power of 2 (i.e., $128 = 2^7$). Since we need the secondary divider to have two outputs of equal frequency and a 90° phase shift between the two, a ring counter is ideal for the output stage of the divider. The states of the ring counter operate in the following manner (shown in Figure 19) where the outputs of these states are gated using OR gates to get the output in a 50% duty cycle format.

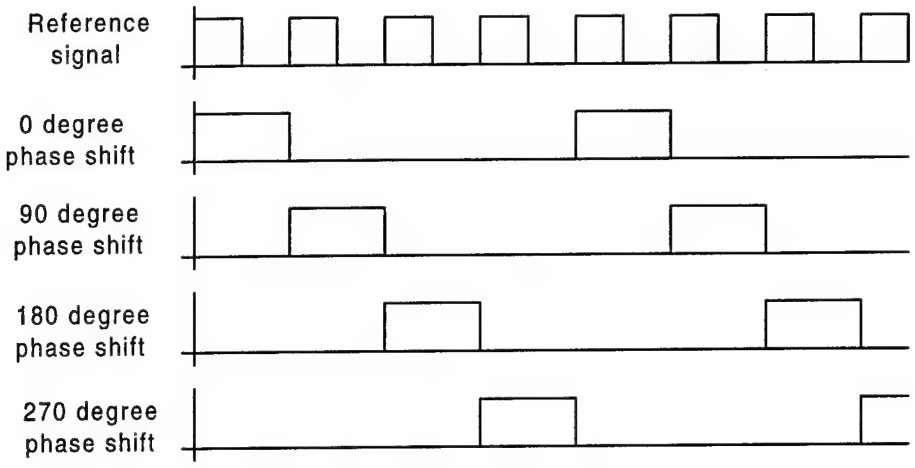

Fig 19. Logic table for divide-by-4 ring counter.

Implementation of this design can be done by either discrete logic chips such as flip-flops or a programmable logic device that operates a state machine. Using flip-flops is reliable but requires rewiring if the output phases are not correct. The programmable logic is more complex and requires a programming language, but it is far more adaptable to change. For the first generation C-probe, I chose to use the programmable logic for two reasons. First, I was not sure on what the final output phases would be based, and I wanted the flexibility to adapt the design without changing the board layout. Second, the current C-probe design utilizes an Altera chip to run the A/D and multiplexing functions of the DC-probe and C-probe. Using the Altera allows me to use the previous programming code for the telemetry section from CADO as well as the program for the ring counter state machine.

Since I need to divide the reference signal by 128, I still needed a 5-bit counter to do the rest of the division. The Altera programming code is equipped with subroutines for N-bit counters. By first passing the reference signal through the 5-bit counter, then the ring counter, I can divide the reference signal by 128 and still be able to pull off the appropriate phases.

The only concern I had about the Altera was its speed. The switching time is rated at 2 ns. This is equivalent to a 2.1° phase shift of the 2.9767 MHz reference signal. This phase shift is far less than I could expect from the filters and multipliers along the main signal path. Actually, I intend to add a phase shift to the reference signal to compensate for all the shifts caused by the devices along the signal path. Adding a phase shift with the Altera is done by adding gates to the input stage. For example, two inverters in series do nothing to the signal except add some propagation delay, which is interpreted as a phase shift by the phase discriminator. This technique will allow me to tune the instrument digitally by adding or subtracting logic gates.

Because of the increase in capability, I chose to upgrade the Altera model from an EP610 to an EP5032. The EP5032 has twice as many input ports, can operate twice as fast, and has twice the number of logic cells used to run the programs.

J. Altera Driver and Pre-Amp

In order to run the state machines and logic gates in the Altera, we need an external clock. This clock needs to run anywhere from about 12 MHz to 48 MHz. The clock is only used to drive the A/D and multiplexing sections of the chip and is independent of C-probe operations. Since there is already an oscillator being used on board, I designed the driver to utilize it. By using the same technology found in the MC12053s, the MC12026A is a divide-by-16 ECL chip. Like the MC12053, the MC12026 can run up to 1.1 GHz and can be programmed to divide-by-8, 9, 16, or 17 through the proper setting of logic inputs. The divide-by-16 will provide a clock pulse of 24 MHz but will be at ECL levels.

The decision to use the Altera requires that the 2.9767 MHz reference signal and 24 MHz clock pulse be conditioned before entering the Altera. Altera technology is based on TTL logic, which means a logic-level-low must be less than .8 volts and a logic-level-high must be

greater than 2 volts. The reference signal, when leaving the divide-by-129, has ECL output levels. As stated before, the only specified logic level in ECL is the peak-to-peak voltage. It is rated at 1 volt p/p. I was unable to find any indication of the offset voltage for ECL so I planned for the ECL signal to be 0 to 1 volt, which later showed to be a problem.

A pre-amp can be implemented with either a simple op-amp configuration or an ECL-to-TTL converter. The ECL-to-TTL converter is very simple to use and I would not have to worry about the appropriate logic levels. The op-amp configuration is not as simple but can be done with parts the lab currently carries. For that reason, I chose to use the op-amp configuration as the Altera pre-amp. For both converters, I chose a non-inverting configuration. However, because the clock driver is at 24 MHz, the AD647 would not have the required gain. Therefore, for the clock driver, I chose to use the AD9618, which has a bandwidth of 150 MHz. This gave me a significant bandwidth margin in case I chose to drive the Altera faster than 24 MHz. The configuration of the two chips is relatively the same and can be seen in Figure 20.

K. Phase Discriminators

The purpose of the phase discriminator is to detect the phase information being carried in the signal path into a voltage that can be sent down through telemetry. The phase discriminator

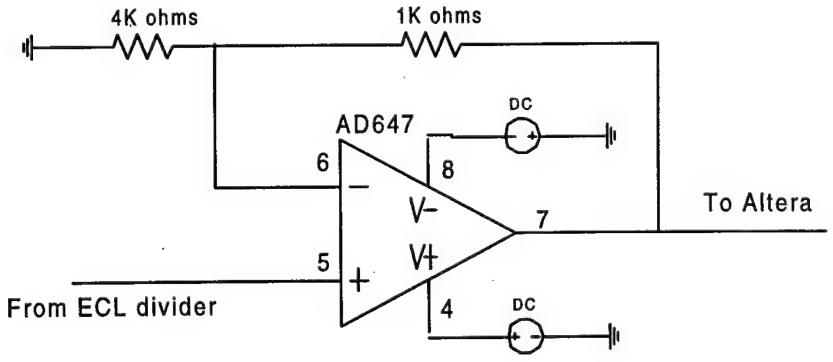

Fig. 20. Altera driver and pre-amp.

operates on the principle that when two signals of equal frequency are multiplied together, the result is a signal with twice the frequency and a DC offset. The DC offset is directly related to the phase shift between the two signals. When the two signals are in phase, the maximum DC offset is achieved. When they are 90° out of phase, the DC offset goes to 0 volts. Using a low-pass filter, all frequency components can be eliminated, leaving only a DC signal that is directly proportional to the phase.

The phase discrimination circuitry has worked well for the previous C-probes so I have duplicated the design with a few changes. The multipliers are AD647s. Since these have a differential output, we need to follow them with a differential filter configuration. Two LF353s have been utilized for this purpose. These are low-frequency op-amps, but since we only need to filter out a 50-KHz signal, they do not have to be very fast.

The one change made to the design of the phase discriminator was to increase the cutoff frequency from 1.4 KHz to 2.0 KHz. This was based on an increase in sample rate of the data from CADO to COORS. An increase of almost 40% in the sample rate meant that we could see higher frequencies, which in turn meant seeing quicker ionospheric phenomena. The changes to the design were done by decreasing the capacitors in the filter from 220 pf to 150 pf. This resulted in the following design (Figure 21). The filter is a two-pole filter. This means that the feedback RC pair must be identical to the input RC pair if the poles are to be located in the same place. Since we are concerned with only the intermediate frequency, there is no reason to design the filter for two different poles.

L. Telemetry Conditioning

The conditioning of the signal for telemetry is dependent on the downlink requirements. The A/D conversion and multiplexing of other signals with the C-probe is based on mission requirements and not the physical restrictions to the C-probe. For efficiency and convenience,

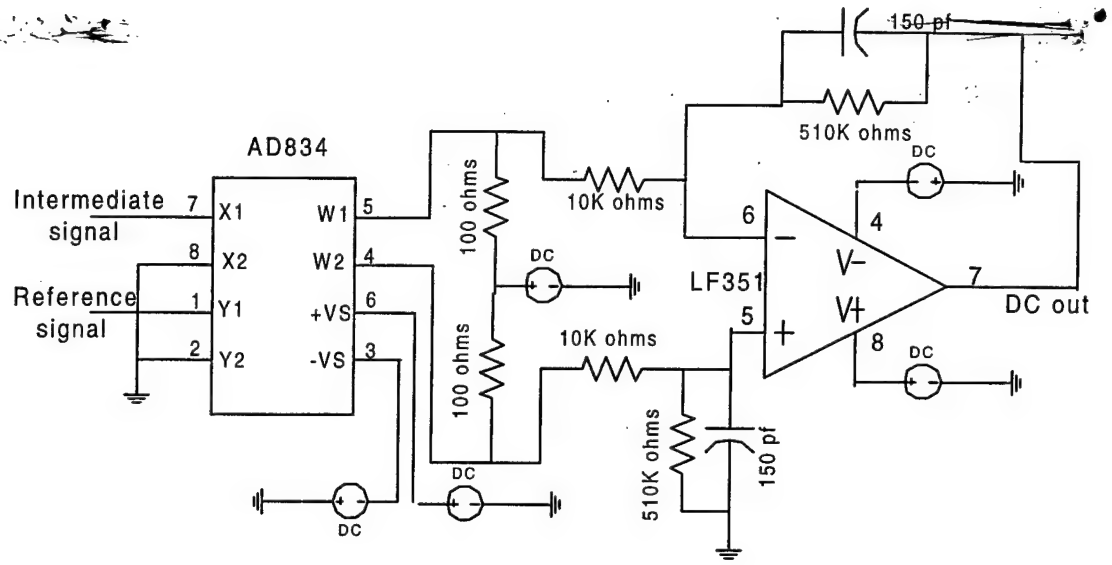

Fig. 21. Phase discriminator.

the Altera is ideal for controlling these tasks and has been used in the past to do so. I made it a point not to overcomplicate the probe and to use as much existing and flight-proven hardware as possible. The only restriction that affects both the telemetry and super-heterodyne system is the cutoff of the output filter. In order to meet the Nyquist requirement for sampling, the highest output frequency allowed is one half the sample rate. However, in order to assure all important changes are being measured through the course of a launch, the lowest frequency the filter can cut off is roughly 700 Hz. Therefore, as long as the sample rate does not drop below 1.4 KHz, the two requirements will not conflict with each other. The expected voltage range is 10 volts, either from 0 to 10 or -5 to +5 volts depending on the particular A/D converters. Either scale will have to same expected resolution of about 2 pf per volt.

CHAPTER IV

CIRCUIT BOARD LAYOUT

A. C-Probe Schematic

The previous chapter described each section of the C-probe design and presented a schematic accordingly. In this chapter, we present the full schematic. I chose to use PCAD to capture the design schematic based solely on the fact that the Space Dynamics Laboratory (SDL) has the resources and experience for using PCAD. PCAD integrates a schematic capture program with a complete circuit board design tool. Appendix A shows the super-heterodyne C-probe schematic.

This schematic was made simply by taking each sub-schematic from the previous chapter and appropriately arranging them so that the flow of the signal was correct. There were essentially no changes in going from the individual schematics to the full schematic. In order to create this schematic in PCAD, the part descriptions and layout foot prints of the MC12053A and MC12026A had to be entered into PCAD's component database.

B. A/D and Telemetry Interface Considerations for Integrating with CADO

A major consideration when designing the full schematic was the A/D and telemetry interface sections. The space allotted on the circuit board for this section is dependent on the launch vehicle's payload space and will dictate the number and types of components allowed. This means that the telemetry interface circuitry is often unique to the particular payload size and launch vehicle. The amount of space that would be allotted for instruments on a Viper-Dart is much less than that of one on a Terrier-Orion launch vehicle, which is the launch vehicle for COORS. The space allotted for the super-heterodyne C-probe is identical to another version of the C-probe that flew as part of the CADO payload. I was able to use the same A/D and

telemetry sections of the older probe for my instrument. In addition, the CADO board had a DC-probe on it, which I chose to keep. Retrofitting the CADO schematic with the super-heterodyne C-probe required two main tasks. First, the old C-probe schematic was physically replaced by the new C-probe schematic. Second, the Altera model had to be upgraded.

Before replacing the old probe, I had to decide which circuits I wanted to keep and which circuit I needed to change. The schematic capture routine in PCAD is not concerned with component placement, wires crossing, and RF shielding issues. Its job is to create a netlist that will be used to check the trace layout section to ensure continuity. However, when using the trace layout routine, we must be concerned with the size board we have to work with, whether ground loops are created by laying new traces, and whether the high-frequency circuits will create too much noise for adjacent components. The problem of restuffing the board is not as simple as filling in the vacant space left by the unused circuits of the old C-probe with the circuits of the new C-probe.

The digital logic required for the new C-probe was more complex than the old CADO C-probe. This required an upgrade of the Altera chip. The pin assignments changed from the old C-probe to accommodate a larger chip. The larger chip allowed all inputs to be placed on dedicated input ports instead of I/O ports. This change made more efficient use of the Altera in the allocation of its programmed tasks. A major difference in the use of the Altera is that it no longer creates the drive frequency. Instead it creates the intermediate frequency. That does not change the fact that the output of the ring counter is sent to the phase discriminator, but it does require a 2.9767-MHz signal from the C-probe to be divided down to the intermediate frequency.

Selecting the Altera's pin assignment is an iterative process. In the PCAD schematic, the inputs are on the left and the outputs are on the right regardless of their physical location on the chip. On the chip, the inputs are at the corners and the outputs are dispersed around the rest of

the chip. Since the placement of the chips on the schematic does not necessarily coincide with their placement on the circuit board relative to other chips, the pin assignments made on the schematic which offer the most legible and organized schematic are often impractical to implement on the circuit board. Only after the chip is placed on the board will the ideal pin assignment and trace connections become evident.

Another responsibility of the Altera is to produce the RF-NOT signal. This signal is transmitted on the opposing pole to the RF drive signal on the dipole antenna. Transmitting an inverted RF drive signal on one half of the dipole antenna along with the normal RF drive signal on the other half will ensure that the spacecraft will stay electrically neutral in flight. The previous probes used the Altera to create both the drive and inverted drive signals. However, since the RF drive signal never enters the Altera in the new design, it is not possible to use the Altera to invert the actual signal as it was done in the past. Therefore, we must find another way to get a 3-MHz signal, which is inverted from the RF drive signal. This is achieved by dividing out the 24-MHz drive clock being sent to the Altera by 8 and then inverting the signal. Since both the RF drive frequency and Altera drive clock come from the same 384-MHz oscillator, their relative phases should not drift away from one another and will always be 180° apart. Using the Altera for this function also means that we do not have to add an ECL inverter to the list of new components. This saves space on the board.

C. Trace Layers and Board Layout

The primary consideration when designing the circuit board for a super-heterodyne system is the interfering effect that the high-frequency components may have on the rest of the circuit board. The noise that might be introduced by the 384-MHz oscillator and ECL dividers must be considered in the design of the circuit boards. Different options for minimizing noise include placing these high-frequency components in a shielded box. This is usually at the

expense of circuit board real-estate. Another option is to place the high-frequency components on a separate board. This option is complicated by the need for transmission lines from one board to the other. Since much of CADO's C-probe design is being kept, I have tried to keep the traces and component placements the same. Appendix B shows the board layout for CADO. The parts that have been eliminated are U2, U3, L1, U12, and associated passive components. The RF Head will be enlarged but still kept on the board, roughly in the same place. The Altera will be upgraded as well and will slightly increase in size. Replacing these components are one oscillator, four surface-mount chips, and three 8-pin op-amps. It is quite apparent from Appendix B that all these chips will not fit in the space vacated by the old C-probe. However, the power board has a lot of free space and room for compaction. The chips that make up the new C-probe do not require any more power supplies than the ones already in use.

This brings up the question of which chips to place on the power board. Since almost all the chips in the super-heterodyne system have either a 2.9767-MHz signal or higher at their input, the issue of transmission line impedances cannot be ignored without a significant change in the current board layout. The most practical method is to place the highest frequencies on the second board and transmit identical or similar signals across the transmission line. This means putting the 384-MHz oscillator and all dividers on the same board. The concurrent dividers would be close enough in frequency that the relative phase difference caused by the transmission line can be kept to a minimum. A 3-MHz signal has a wavelength of 100 meters. A 2.9767-MHz signal has a wavelength of 100.8 meters. This means that if the transmission lines are of equal length, the difference in impedance between the two lines would be .8%. This is far less than the expected phase shift induced by any of the other sections along the rest of the signal path. Another advantage of placing the high-frequency components on the power board is that there is enough space to place a shielded box around this section as well as the ECL-to-TTL op-amp

converter used to drive the Altera's clock. This will add to the protection as well as allow for a sufficient amount of space on the main board to implement the rest of the super-heterodyne design. The high-frequency section was broken up into two sections. The first section has the 384-MHz oscillator and concurrent dividers. The second has the ECL-to-TTL op-amp converter. This chip is separated from the others to first shield it from the oscillator and second to shield the concurrent dividers from it. Appendix C shows the power/high-frequency board layout. Careful attention was made to keep the traces from the oscillator to the dividers as short as possible. Also, a large enough gap was left between the two sections so that a shield could fit between them.

With the high-frequency section on the power board, that left one surface-mount chip and two op-amps left to fit on the main board. Before placing these chips on the board, I increased the spaces for both the RF Head and the Altera. Because the Altera's model was changed, the old wiring was obsolete. As for the RF Head, the biggest concern was getting the 3-MHz RF drive signal close to the head. This ensured the shortest transmission length and the least possibility of getting noise into the signal. Also, the 2.9767-MHz reference signal and 24-MHz clock signal needed to enter the board close to the Altera for the same reasons. Once these issues were settled, the rest of the chips could be placed.

The RF Head post-amp was placed near the RF Head to reduce the possibility of noise getting into the small signal output of the head before being amplified. The reference signal's pre-amp was placed near the Altera so that the high frequency signal would not interfere with other components as the trace passed by them. As for the intermediate multiplier and filter, having them in close proximity was ideal but not a priority. Ironically because of the tight area I had to work with, all distance requirements were easily met. Appendix D shows the placement of the components for the main board. The trace layers for the main board were rather

straightforward. The Altera provided the biggest challenge. The pinouts from the previous chip were much different than the new chip. This meant that the traces had to be redesigned. As stated earlier, it took an iterative process to come up with the final design for the Altera's traces. When drawing the traces, I had two main concerns. First, I wanted to limit the number of traces passing beneath the chip. Second, I wanted to keep the input pins at dedicated inputs and not have to use an I/O port. To solve this problem I categorized all the chips and ports that the Altera had pins assigned to, by which side of the chip they were on. Then by first determining the chips with dedicated inputs, I placed those traces. Then I arranged the I/O ports so that no traces had to cross one another and only a few had to cross beneath the chip. The result of the trace layout for both boards can be found in Appendix D. The traces in Appendix D are categorized into signal and power traces. The thicker lines are the traces that carry power across the board. The thinner lines carry the signals. The traces were carefully plotted so that they never made a turn greater than 45° unless they were at a pad. This was done so that the high-frequency signals would not radiate at sharp bends in the trace.

CHAPTER V

CONSTRUCTION, TESTING, AND DESIGN REVISIONS

A. Implementation of Design

This chapter documents the process of constructing and testing the designs presented in Chapter III, and the revisions made to these designs. I systematically go through each section of the super-heterodyne C-probe and discuss what the problems and successes were when implementing the preliminary design found in Chapter III, and finish each section with a final subsection schematic as needed as well as document the output of these sections. These final designs are based on changes made after observing the performance of the original design and making the required changes to ensure the proper function of the design.

B. 384-MHz Oscillator

Implementing the 384-MHz oscillator was very easy. Since the ECL output levels were designed into the package, the construction was completed by simply soldering the package onto the printed circuit board. During the probes testing phase, I soldered individual socket pins into the pads and placed a 400-MHz oscillator into these pins. We purchased the 400-MHz oscillator along with the two 384-MHz oscillators for testing purposes. This way, if I burned out the oscillator during tests, I would not be burning out flight hardware and could easily remove it from the board since it was not soldered. The final task in construction was to pull off the socket pins and solder a 384-MHz oscillator to the board.

Ensuring that the oscillator was working required two separate tests. First, I tried using an oscilloscope. Unfortunately, the bandwidth was half that of the oscillator and the output signal was very difficult to see. The amplitude was decreased by a factor of 10 from what we expected and the shape of the waveform was more sinusoidal than square. All of these were

expected because of the bandwidth limitations. Since I did not have access to an oscilloscope with a higher bandwidth, I chose to connect the concurrent dividers and use them as a test-bed to see if the oscillator was working.

C. Divide-by-128/129

The two concurrent dividers provided an exact and stable output. Since the oscillator was at 400 MHz, the divide-by-128 showed 3.125 MHz and the divide-by-129 showed 3.10078 MHz. These were as exact as the precision of the frequency counter allowed. These outputs showed that both the crystal oscillator and concurrent dividers were working within expected parameters. The only surprise was the offset levels of the ECL signals. The following figure (Figure 22) only shows the output of the divide-by-128. Since the two signals are so close in frequency and the offset voltages are equal, I felt that only one output was needed to illustrate the dividers' output. The frequency of the waveform in Figure 22 is at 3 MHz and the peak-to-peak voltage level is 1 volt as predicted, but the DC offset is a surprise. The logic level low is at 3.5 volts and the logic level high is at 4.5 volts. This means that the ECL-to-TTL op-amp converter must subtract 3.5 volts and multiply the result by 5. The standard logic level specification for

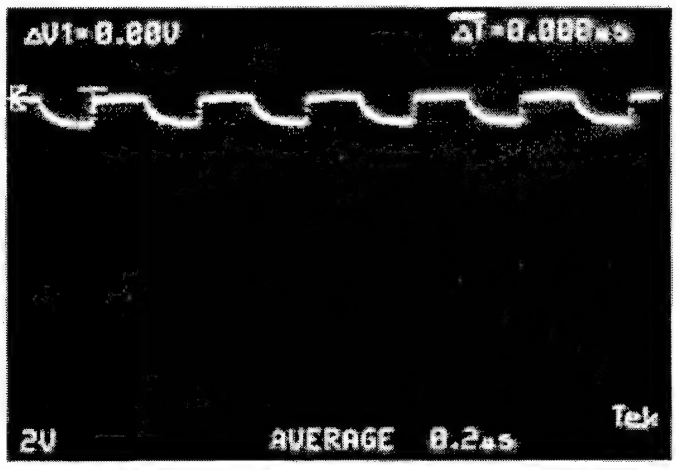

Fig. 22. Divide-by-128 output.

ECL is a logic level of -.8 volts and a low of -1.8 volts. This is assuming rail voltages of -5 and 0 volts. Observing the output of the MC12053A, I would surmise that ECL logic levels are based on the rail voltages and generally follow the rule that the logic high is roughly equal to .5 volts below the upper rail and the logic level low is 1 volt below that.

Conditioning these signals for transmission from the power board to the main circuit board requires a simple coupling capacitor of about .1 μf. Since the RF drive signal requires a 1 volt p/p signal with no DC offset, the output of the divide by 128/coupling capacitor series can be directly fed into the RF Head. On the other hand, the reference signal has to be conditioned with an op-amp in order to drive the TTL of the Altera. Instead of requiring the op-amp to offset the signal by 3.5 volts, I chose to add the coupling capacitor in series so that the offset would only be .5 volts. The transmission lines for the antenna drive signal and reference/local oscillator signal from the power board to the circuit board are coax cables. Coax cables help to prevent ground loops and noise from affecting the transmission of the signal from board to board, while at the same time preventing the transmitted signal from affecting any of the other circuits.

D. RF Head

The RF Heads for C-probes have changed in size since their premier. The original design consisted of a large ferrite core encased in a protective shield. As the rockets grew smaller, so did the allotted payload space. This caused the ferrite cores to decrease in size to accommodate the changes in space. The size and purity of the ferrite core material is responsible for both the amount of RF noise allowed to enter the circuit through the head, and the efficiency of the transformer. The larger the ferrite core is, the greater the magnetic flux is between the two windings and the more efficient the transformer. Because the size allotted on COORS for the RF Head was substantially larger compared to previous flights, I increased the ferrite core size by combining three cores [7]. The implementation of the current transformer was done using the

following technique shown in Figure 23. This particular design steps up the voltage from the antenna drive wire that passes through the center, to the windings around the core, which lead to the RF Head post-amp. A perfect transformer would step up the voltage across the windings preserving the waveform's shape, but because of the 3-MHz square wave input signal and the inductor created by the windings around a ferrite core, the true output of the RF Head is seen in Figure 24.

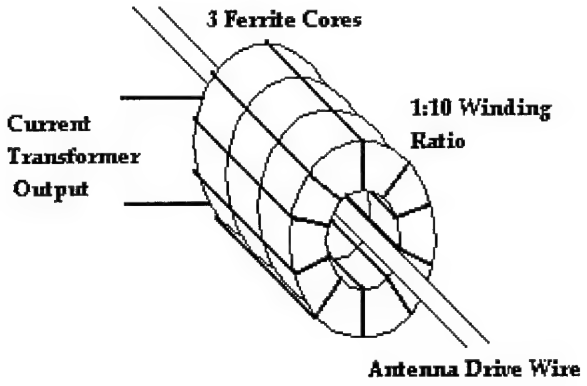

Fig. 23. Current transformer.

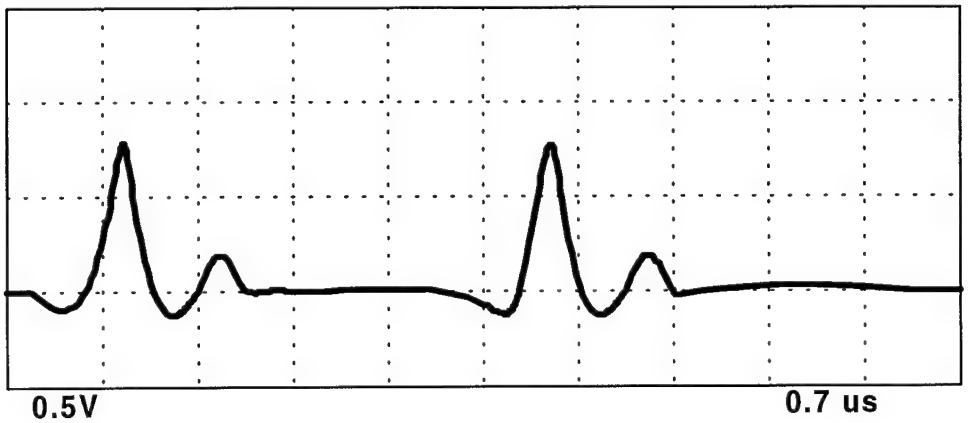

Fig. 24. Output of the RF Head.

From Figure 24, we can see that the square wave that entered the RF Head is not the same signal coming out. The fundamental frequency is identical but the shape is much different and the size is significantly decreased. This indicates a poor frequency response at 3 MHz.

The full RF Head has two transformers with the secondary coils in series. In order for the RF Head to be effective, both transformers must be constructed so that they are identical. This will insure that at initial conditions, the phase measured will be 0°, tuning out the free space capacitance term from the RF Head. Also, if the transformers are not identical, as the measured capacitance changes during flight, the measured phase difference will be a combination of both the difference in inductor values for the transformers as well as the change in measured capacitance. The difference in transformer inductance comes from both the difference in the core's flux potential and in the wire loops. If we assume the manufactured cores do not differ significantly from each other, the wire loops will dictate how similar the transformers are. The more evenly spaced each loop is, the better chance there is of building two identical transformers.

E. RF Head Post-Amp

The purpose of the RF Head post-amp is to amplify the small signal leaving the RF Head. Using the non-inverting design found in Figure 14, I was unable to achieve the gain needed with the AD647 so I investigated other chips. My main criterion for the new op-amps was the small signal bandwidth. Settling on the AD9618, I designed a similar amplifier shown in Figure 25.

Testing the op-amp configuration was done by first using a function generator to test a bread board implementation. At 3 MHz, the function generator could only handle a sinusoid, but was sufficient to measure the gain of the amplifier. I found that the gain was slightly over 20 v/v and chose to implement the design on the circuit board.

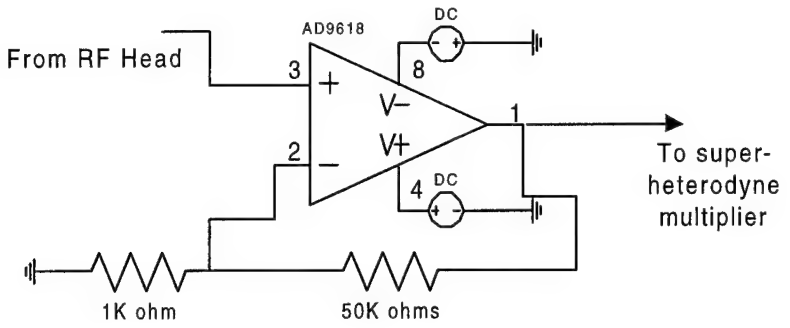

Fig. 25. RF Head post-amp.

Originally, there was no intent to filter the output, but with the spikes seen in Figure 24, I decided some level of filtering was necessary. Using the basic RC filter equation below, I chose a capacitor value of 2 pf.

$$f_c = \frac{1}{2\pi RC} \qquad \textbf{(5 - 1)}$$

The resistor value in the equation is the 20-kΩ feedback resistor from the original design. Using the equation above, a 2.6-pf capacitor is needed for a 3-Mhz filter. Unfortunately, the only values of capacitor available were 2 pf and 3 pf. Since this capacitor was not included in the original design, I had to add it to the board externally. Because of the limited space, I could only fit one capacitor and chose to use the 2-pf capacitor. The 2-pf capacitor and 20-kΩ resistor create a cutoff frequency of 3.97 Mhz. The output of the final amplifier/filter is seen in Figure 26.

I was quite pleased with the output. The level of noise was small compared to the output of the RF Head post-amps on previous probes, and the amplitudes of the higher harmonics appeared to be filtered to the point where the intermediate multiplier and filter could filter out the rest of the high-frequency noise.

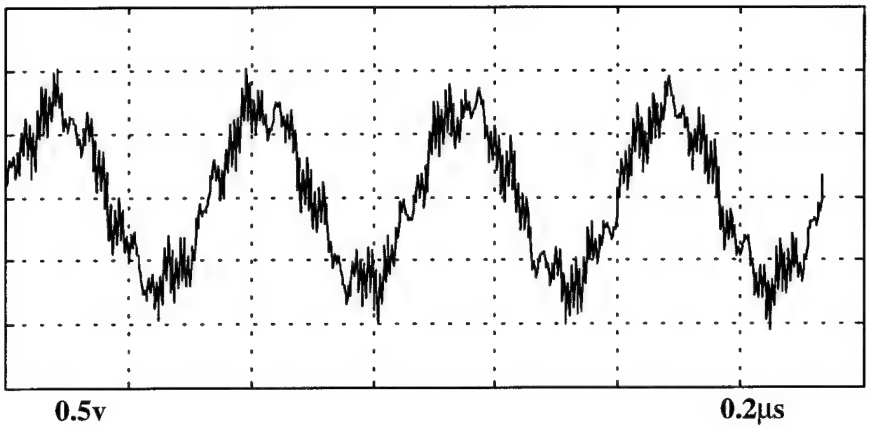

Fig. 26. RF Head post-amp output.

Through the initial stages of testing, the power was supplied via external power source. These sources had low noise levels and could handle relatively high current requirements. For flight, the power is supplied through DC-to-DC converters. These converters have imbedded switching logic that often creates noise that propagates throughout the entire system. When I implemented the converters, the op-amp configuration in Figure 25 no longer produced the output found in Figure 26. Instead it produced a 66-MHz sinusoid. At first I thought it was a filtering problem, but after placing the chip back on the bread board and trying different resistor configurations, I discovered that the chip had gone into a state of uncontrolled oscillation. It was at this time I began to investigate the chip's data sheets more thoroughly.

Originally, when I selected the AD9618, I looked only at the bandwidth specifications and the implementation diagrams. The bandwidth was at 150 MHz, which was more than enough and the implementation diagrams were identical to standard inverting/non-inverting amplifier configurations. However, because the diagrams showed the configuration I expected for an amplifier, I never looked at the gain equations until after I had the problem with the op-amp oscillating. The op-amp is actually a trans-impedance amplifier, which has restrictions on the resistor values. The feedback and input resistors are actually used for both gain and filtering.

The following transfer function dictates the gain and filtering characteristics of the amplifier for the non-inverting configuration.

$$\frac{V_{out}}{V_{in}} \approx \frac{1+\frac{R_F}{R_I}}{s\tau\left(1+\frac{R_S}{R_I}\right)+1} \qquad \textbf{(5 - 2)}$$

where

$\tau = \left(1 \cdot 10^{-12}\right) R_F$

R_F **is the feedback resistance**

R_I **is the input resistance**

$R_S = 75K\Omega$

The data sheets also specify that feedback capacitors should not be used on the AD9618. Instead, the ratio of the resistors is responsible for the filtering. Ironically, I plugged in the resistor values I used for the initial design into Equation 5-2 and found the gain to be .7 v/v at 3 MHz. At all frequencies below about 100 kHz, the gain was around 20 v/v. I am unable to explain why the chip worked as well as it did before the DC-to-DC converters were added, but since the chip went into oscillations after the converters were added, I thought that using the chip as it was originally designed for would be the safest way to insure a successful probe. The following set of guideline equations was provided by the data sheets for determining R_f and R_i. Since the non-inverting transfer function was unable to handle the gain, I chose the inverting amplifier.

$$R_F = 1100 + 8G \qquad \textbf{(5 - 3)}$$

$$R_I = \frac{1100 + 10G}{G} \qquad \textbf{(5 - 4)}$$

where

G is the Closed - Loop Gain

The two equations above indicate that there is a specific set of resistor values resulting in a specific gain. This is a departure from the standard ratio-driven amplifier gains. Using a gain of 20, I calculated R_f and R_i to be 1260 Ω and 65 Ω, respectively. This resulted in the following RF Head post-amp configuration shown in Figure 27. The resultant output of this post-amp is shown in Figure 28. The output still has a significant level of oscillation at 66 MHz, but the 3-MHz component was present and strong enough to be effectively filtered from this signal in the intermediate multiplication and filtering section. I chose to keep this signal and filter out the 66-MHz oscillation in the intermediate filter section.

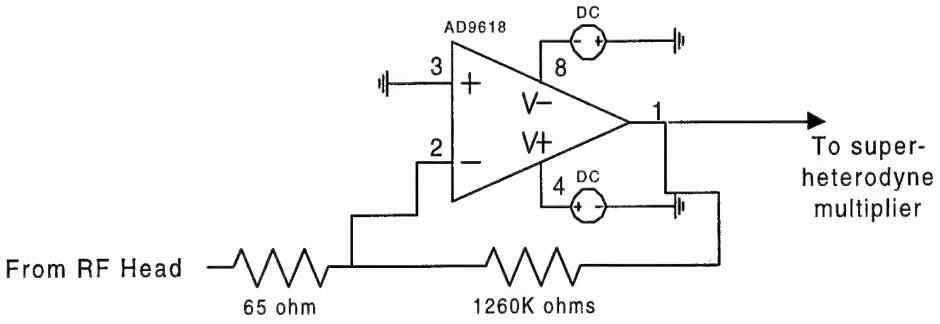

Fig. 27. Final RF Head post-amp configuration.

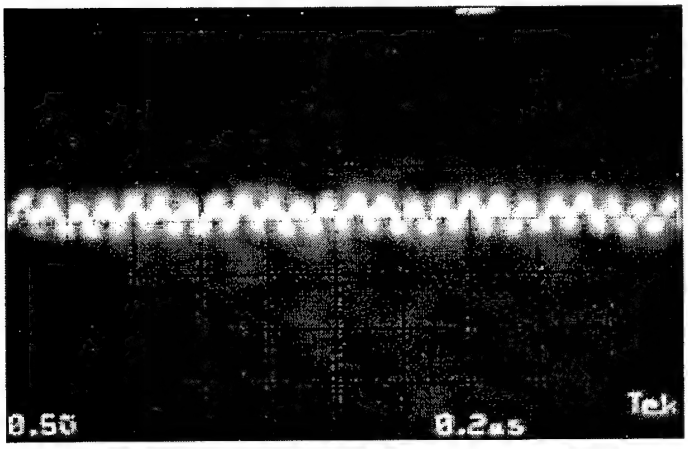

Fig. 28. Final output of RF Head post-amp.

F. Intermediate Multiplier

With the output of the RF Head post-amp within expected limits, the task of the multiplier is simply to multiply the 3-MHz output of the RF Head and the 2.9767-MHz output of the divide-by-129 chip. The AD 835 4-Quadrant multiplier has an added feature that can multiply the output of the multiplier by a constant. This constant can be set anywhere from .9 to 1.1. I chose to keep it at 1 for the sake of simplicity. The multiplier also has strict input limits, which are that the input voltage levels cannot exceed ±1 volt.

During the initial design, before the DC-to-DC converters were added, the output of the RF Head post-amp was 1.2 volts. The resultant output of the multiplier was a DC value of 5 volts. Since the AD835's literature never stated the effect of exceeding the input limits, I can only assume that saturation is the standard result. This required me to reduce the gain of the RF Head post-amp so that the output signal (the input to the multiplier) was below 1 volt. This summarily fixed the problem and I was able to achieve the following output (Figure 29). However, when the DC-to-DC converters were added, the characteristics of the entire circuit changed again. The result was an excessive amount of noise in the circuit. The multiplier was still able to multiply the two signals, but the high-frequency noise caused the output to be

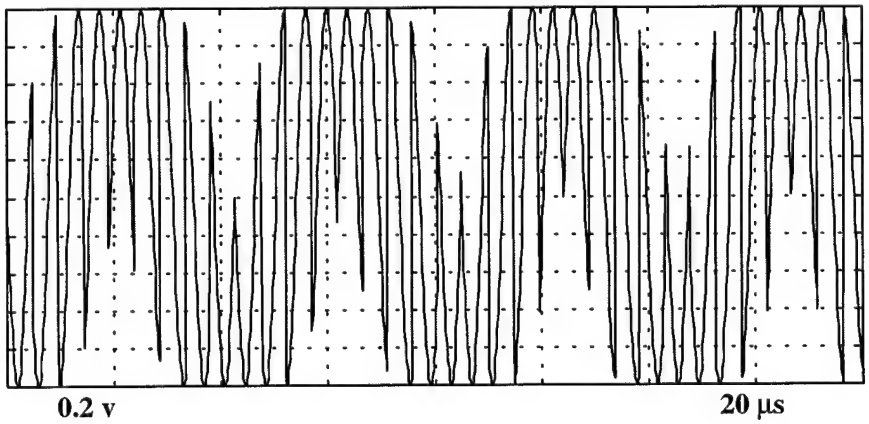

Fig. 29. Preliminary output of intermediate multiplier.

modulated. The noise that is introduced by the DC-to-DC converters causes the trans-impedance amplifier to oscillate slightly. Since this is common mode for the post-amp, it cannot be filtered out by the post-amp. This means that another filter in series must accomplish this. If this were the case, I would be stuck with the same problem of finding a chip with the bandwidth. The other option is to filter out this high-frequency noise after the multiplier in the intermediate filter. The problem with that method is that it must first pass through the multiplier, causing the output to be overmodulated. I chose to use the intermediate filter because the frequency components I needed would still be inherent in the signal. As long as the filtering was sufficient, the 23.255-kHz signal could still be retrieved.

Driving the intermediate multiplier with the 2.9767-MHz signal directly caused some problems with the input stage to the multiplier. In order to get the ECL signal's DC bias down, I used a decoupling capacitor. Unfortunately, the MC12056A was unable to drive both the Altera and AD835. Therefore, since the 2.9767-MHz signal is used to drive both the intermediate multiplier and the Altera, I chose to send it through the Altera first and use the Altera as a buffer for the multiplier. This was done by simply programming the input signal directly to an output port and following it with a decoupling capacitor to cut any DC offset and a voltage divider to reduce the peak-to-peak voltage to 2 volts.

G. Intermediate Filter

The intermediate filter was originally designed as a band-pass filter around 23.255 kHz. Although the filtering of the higher frequencies was successful, I was never satisfied with the slope of the phase response around the cutoff frequency. The possibility still existed that somewhere in flight, the filter could drift, causing the signal to change 180°. Without any way to

tune the filter in flight, this could cause the output to jump off scale. The output of the band-pass filter, before the DC-to-DC converters were added, is shown in Figure 30.

The output shown in Figure 30 is ideal in frequency for a super-heterodyne system, but I wanted to see if I could simplify the circuit and still get the same filtered output with less modulation. The first configuration I tried was a simple non-inverting amplifier with a gain of 1. The result was the same as shown in Figure 30. This was a clear indication that the bandwidth of the op-amp was doing most of the filtering. The op-amp for the intermediate filter was an AD647. With a specified bandwidth of 1 MHz, the 6-MHz component should be reduced by almost 10% from the op-amp alone. With a gain of 1, the intermediate filter became both a buffer and a filter. These results were very promising going into the phase discriminator. The signal was clean and sinusoidal, which greatly simplifies the phase discrimination process.

As with all the sections previous to this one, when the DC-to-DC converters were added, the signal path became very noisy. I now had the task of filtering out the high-frequency modulation and the 6-MHz component from the intermediate multiplier output. Since the filter was in the non-inverting op-amp configuration, there was no active filtering besides the inherent

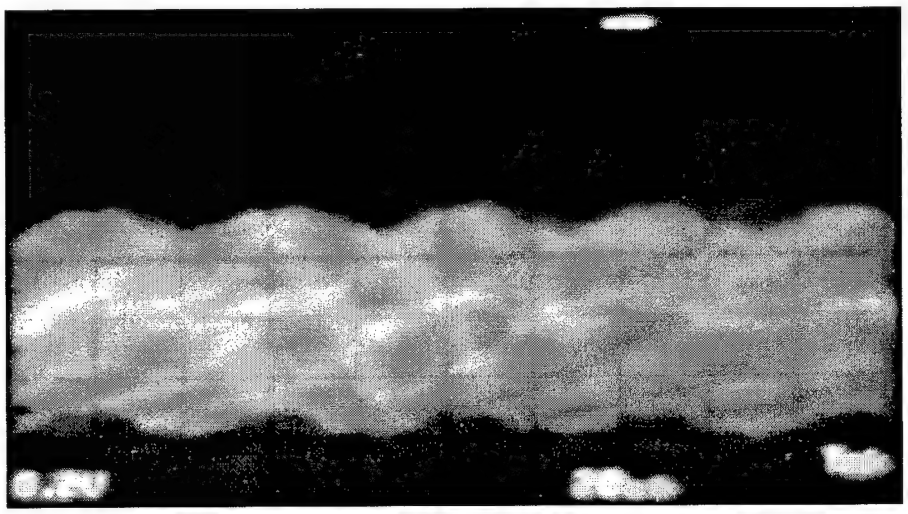

Fig. 30. Preliminary output of intermediate filter.

bandwidth of the op-amp. In order to build the active filter, I converted the op-amp to a non-inverting amplifier and added a feedback capacitor for filtering.

The first attempt at the intermediate filter with DC to DC converters had a gain of -1 v/v with R_i and R_f, both at 100 kΩ and the feedback capacitor at 66 pf. The amplitude of the output was 100 mv and did not have the amplitude needed to complete the phase discrimination. To increase the gain, I decreased the input resistance. This allowed me to keep the RC pair for the feedback filter so that the cutoff frequency would not change. I decreased the input resistance to 10 kΩ, which resulted in the following output (Figure 31). Although all the modulation has not been filtered out, the filter in the phase discriminator can clean up the signal. Because the intermediate frequency is so low compared to the high-frequency noise, the multiplication procedure used in the first step of the phase discriminator will not cause the current signal to be infected with the noise. Instead, the high frequencies will wrap around 0 Hz and settle high in the frequency spectrum. With the phase discriminator's filter set around 1 kHz, a one-pole filter will decrease the high-frequency noise by more than 60 dB or .001 v/v.

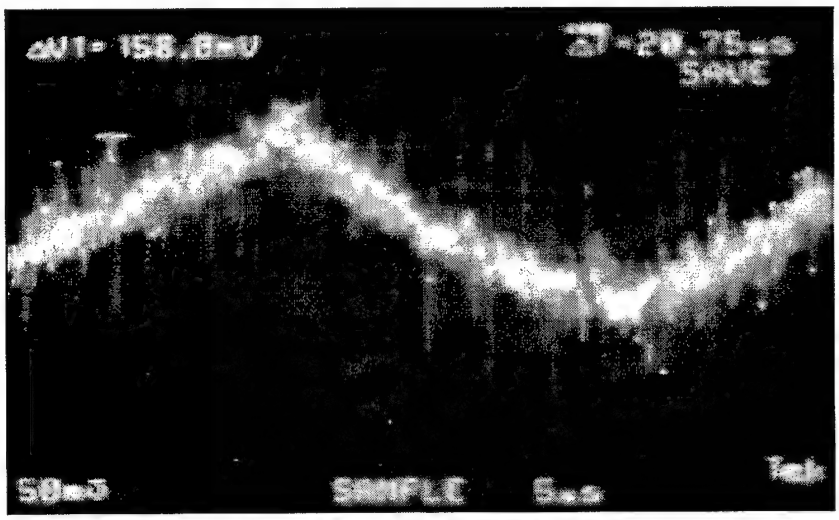

Fig. 31. Final output of the intermediate filter.

Another benefit to this design is the limited gain utilized with the amplifier. If needed, the gain can be increased by a factor of 10. Increasing the gain of the intermediate filter is equivalent to increasing the resolution of the system. For this reason and the filtering considerations above, I chose to keep this filter design seen in Figure 32.

H. Secondary Dividers

The construction of the secondary divider section was completed with Altera programming logic. The divide-by-32 and divide-by-4-ring counter were both implemented as state machines using a programming language unique to Altera. The key difference between the previous C-probes' Altera programs and the super-heterodyne model's Atlera program is the frequency at which they operate. Previous probes used the Altera to create the drive frequency for the RF Head while the current model uses the Altera to operate on that signal to condition it.

The conversion of the old C-probe program to the new model requires the addition of the 5-bit counter as seen in Figure 9. First, the 5-bit counter is programmed to trigger off the reference signal input instead of the Altera's clock input. The 5-bit counter utilizes a module found in the programming language that simplifies the implementation of an n-bit counter. The

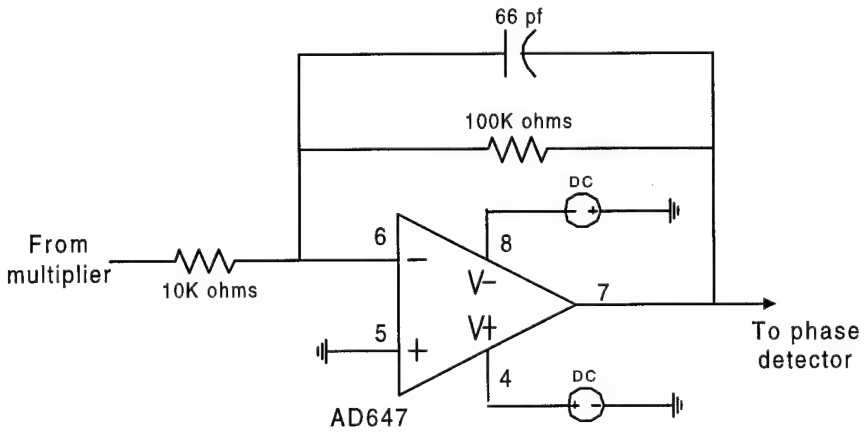

Fig. 32. Final intermediate filter design.

module will create a counter n-bits long and allow the user to access any of the n-bits. By accessing the final bit of the 5-bit counter, and using it as the trigger for the 4-ring counter, the resulting division value for the secondary divider becomes 128 (32 x 4). This method allows the secondary divider to divide by a large number such as 128 while at the same time having four outputs of equal frequency, but offset from each other by 90°. The full Altera program can be found in Appendix E.

During the testing of the Altera program, I ran into a serious phasing problem. Since my only output source was the two outputs of the 4-ring counter, I had to judge the success of the secondary divider based on these two outputs. The primary concern was whether or not the phases of the two signals were 90° apart from each other. Measuring the outputs on an oscilloscope showed that they were always 90° apart in phase, no matter how many times I cycled the power to the Altera. However, when I brought the phase discriminator on line, I found that the DC outputs of the discriminator changed randomly with time. I hypothesized that the changes in the DC levels came from the Altera because the changes were discrete and the Altera was the only discrete logic in the signal path after the concurrent dividers. The sudden changes were most likely caused by the Altera changing states, but I could not determine why this was taking place. Finally, after hours of searching, Wayne Sanderson, the lab technician, found the problem. The soldering iron was on the same power strip, as the DC power supply that supplied the +5 volts to the Altera. As the soldering iron automatically switched on and off based on its mechanical thermostat, it sent a spike through the power strip, which caused the Altera to skip states. The reason this did not appear at the output of the Altera when I measured the relative phases was that the relative phases never changed between the two outputs. They were always 90°, but the relative phase between the 23.255-kHz reference signal and the 23.255-kHz intermediate frequency changed.

This event caused alarm when it occurred. It put the C-probe's stability in serious doubt. I was not sure if the spikes inherent on the DC-to-DC converters would have the same effect on the circuit. Fortunately, when I implemented the converters, the Altera never changed states once it was on. However, another problem presented itself when I was testing the Altera's stability. When the power was turned on to the Altera, the relative phases between the Altera's output and that of the main signal path were never consistent. Every time the power was turned on, the DC output levels of the phase discriminator would change by as much as 75% of full scale. This meant that the Altera was never restarting in the same state relative to the RF drive signal. This was never a problem with the previous probes since the Altera created both the RF drive and reference signal from the same clock. The problem with the random start-up states is most likely caused by the 5-bit counter. Since there were more than four different configurations, it was clear that the 5-bit counter was causing the problem and not the 4-ring counter. A 5-bit counter can create up to 32 different start-up states relative to the RF drive signal. Even though the Altera starts up with all its states at 0, if it does turn on at the same rate each time, the resultant phase difference between the intermediate and reference signals will be random.

I am confident that the super-heterodyne system will work even under these conditions. However, some resolution will be lost since the probe must be built to handle any of the possible outputs. Tuning becomes pointless since the phases change at each cycle up. Also, since there are so many options, it is not practical to recycle the power on the launch pad until an ideal initial condition is met. The problem of resolution will be discussed more in the calibration section.

I. Altera Pre-Amp

Implementing the Altera created another problem besides randomly shifting states. The Altera's inputs from the high frequency section were ECL levels while the Altera requires TTL

levels to operate. This was considered in the design section and planned for with two pre-amps. The first pre-amp conditioned the 24-MHz input clock while the other conditioned the 2.9767-MHz reference signal. Unfortunately, both designs failed but for different reasons.

The first problem came early on in the circuit board's construction. When I was building the high-frequency section, I had all the surface-mount chips soldered at the same time. This included the MC12053As, the MC12026A, and the AD835. Since the three divider chips were all dividing the same signal, I decided to test them together. Both of the MC12053As worked very well. However, I was only able to get a DC output as a response from the divide-by-16. The voltage level was at 3.5 volts, which is the logic level low for the ECL chips on the board. This was my first experience with ECL so I was unsure of what the problem could be. I was able to ascertain that since the output was at a standard logic level for the chip, it was not necessarily destroyed or burned out. I hypothesized that since the output stage did not seem to be damaged, it was most likely a problem with the input stage or input signal. The data sheets for ECL/MECL only specify a difference between the logic level high and logic level low. The applications engineer at Motorola informed me that the logic levels for ECL are based on the rail voltages. Since I was operating the rails of the MC12026A at 0 and 5 volts, the logic levels should be 3.5 volts to 4.5 volts. I was not able to check the output levels of the oscillator since the oscilloscope's bandwidth only extended to 200 MHz. I used the outputs of the MC12053As to verify this. The first alteration I made was to the oscillator. I created a voltage divider that was used to reduce the DC offset of the oscillator's signal. I ran the DC offset level from 4 volts to 2 volts with the voltage divider, all the while using the MC12053As as an experimental control. The concurrent frequency dividers failed when the DC offset level dropped below 3.2 volts. I continued decreasing the DC offset down to 2 volts to ensure that the divide-by-16 was not built to operate at a different level than the divide-by-128/129. Once I was satisfied that the input

level into the divide-by-16 could not be changed to result in the proper operation of the chip, I researched other designs for dividing the 384-MHz signal down to 24 MHz.

Finding another divide-by-16 ECL chip was complicated. I was able to find an abundant supply of divide by 4s and 8s as well as divide by 32s and 64s. Therefore, I was forced to put multiple dividers in series. I was also restricted by space and speed. I could not use surface-mount since that would require the refabrication of the board. Requiring dip chips meant the speed that many of them would work at was greatly reduced from that of the surface mount technology. Ultimately, I chose to start with a single flip-flop as an input stage to do the divide by 2 and then follow it with a 4-bit counter chip. The 4-bit counter would not work above 200 MHz and with the input frequency at 384 MHz, an input stage was needed to divide the frequency down below 200 MHz. This meant that only 3 out of the 4 bits in the counter were needed. The Mmc12090 was chosen for the divide-by-2 stage because of its 750 MHz bandwidth while the MC10H016 was chosen as the 4-bit counter. Since I was implementing new chips, I decided to add an ECL-to-TTL converter to the series instead of using an op-amp in a summing configuration. The resultant Altera driving circuit can be found in Figure 33.

The new design for the Altera driver was plagued with the same problems as the MC12026A. The ECL chips were not being successfully driven by the previous states. I was able to get the MC12090 to divide the 384 MHz signal down to 192 MHz, but the MC10H016 would not divide that signal by any value. I implemented the ECL-to-TTL converter on a

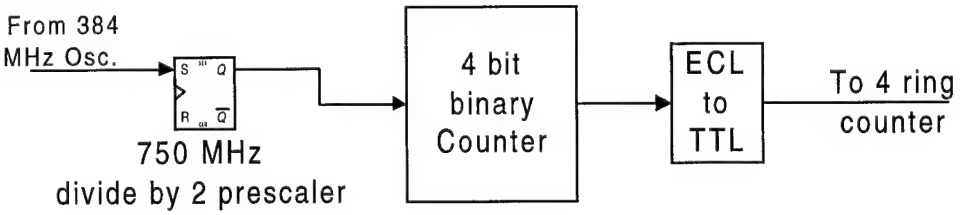

Fig. 33. New Altera driver configuration.

breadboard and drove it with a 100-KHz ECL signal to determine if it had the same problem. I was unable to get any ECL-to-TTL conversion from that chip either. At this point I abandoned any attempt to get the 384-MHz oscillator to drive the Altera and bought a 12-MHz crystal oscillator that drove the dedicated input clock for the Altera. Since the dedicated input clock is only used to drive the A/D logic on the board, the dedicated input clock does not necessarily have to be in phase with the 2.9767-MHz signal. This simplifies the design by replacing the divide-by-16 and Altera pre-amp with a single crystal oscillator.

There is another pre-amp required for the Altera. This is the pre-amp from the 2.9767-MHz signal to the Altera. Since the ECL to TTL converter did not work, I chose to use an op-amp in a summing configuration. Using an AD9618 was somewhat more complicated mathematically, but the premise was the same as a standard op-amp. The AD9618's bandwidth is dependent on the resistor combination. However, since a DC signal is at 0 Hz, the required bandwidth is 0. This means that I can set the bandwidth with the resistor combination for the 2.9767-MHz signal and simply add whatever input resistance is needed for the DC signal. The result is a 2.9767-MHz TTL signal. This configuration for the pre-amp is shown in Figure 34.

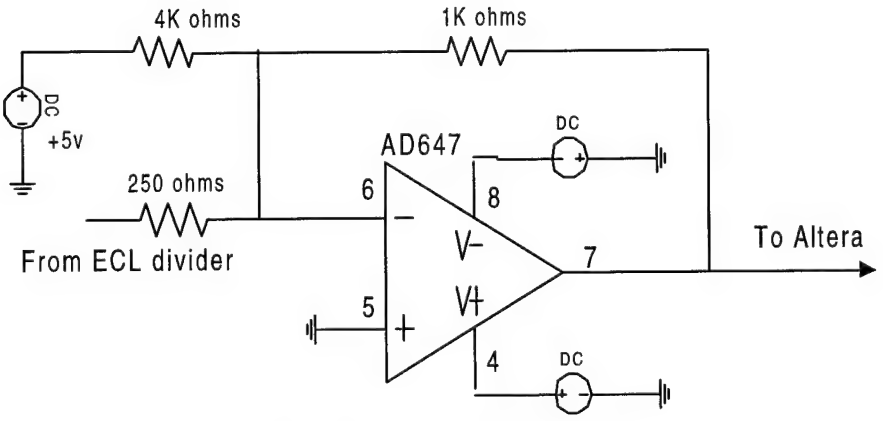

Fig. 34. Reference signal Altera diver.

J. Phase Discriminator

The design of the phase discriminator did not change much from the previous probes. The biggest difference was in the bandwidth of the filter included in the discriminator. As shown in the design section, the discriminator consists of a multiplier and filter. The implementation of the multiplier was identical to the previous probe designs while the feedback resistor/capacitor combination in the filter changed. Testing the multiplier had to be done with either a difference probe since the multiplier was a difference multiplier or by measuring the output of the filter. I chose to go with the full implementation since this was a proven design.

Although the design of the discriminator did not change, the output of the Altera was different from the previous designs. These designs used the reference signal as a gating signal. The output was from 0 to 1 volt instead of from -1 to 1 volt. This DC offset in effect causes the output of the multiplier to have components at 0, 25, and 50 kHz. This complicates the filtering process by requiring the filter to attenuate a signal at half the frequency of the targeted 50 kHz. I chose to add a decoupling capacitor to the output of the Altera so that there would not be a 25-kHz signal and the DC component would solely be produced by the difference in phase and not from the contribution made by the reference signal. This being the case, the only other difference is in the resistor/capacitor combination I designated in the design section. The following output signal illustrated in Figure 35 is the output of the discriminator.

Figure 35 shows by the ripple found in the output that not all of the 50-kHz signal was filtered out by the phase discriminator's filter. This means that either the filter must get sharper or digital filtering must be used after the launch. Since the utilization of a higher order filter would require a refabrication of the board, I chose to leave the 50-kHz frequency segment in the telemetry and deal with it in data reduction.

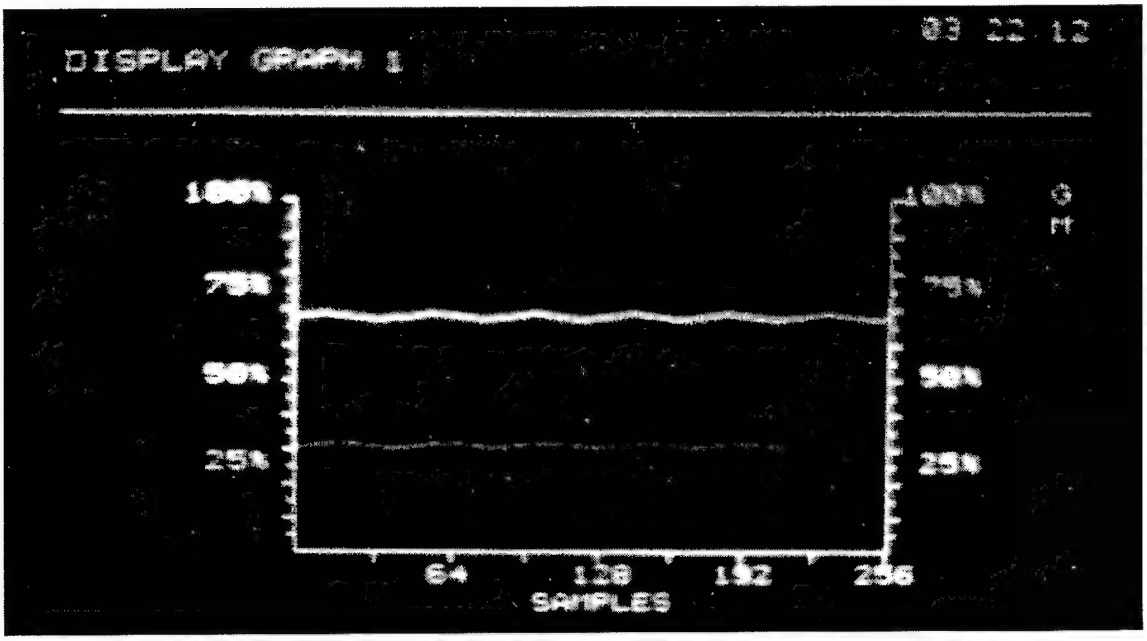

Fig. 35. Phase discriminator output.

K. The A/D Section and Telemetry

The rest of the design was taken directly from the CADO payload specifications. The only difficulty I found in implementing this configuration was with the Altera program. The old C-probe used the EP610 chip where as this system used the EP5032. The program from the EP610 was not fully compatible with the EP5032. The previous program defined the dedicated input clock as a global variable. The current model would only recognize it as a node. This problem only showed up in the A/D section since the super-heterodyne system never uses the dedicated clock for any of it processes. Once this problem was fixed, the telemetry worked to the proper specifications.

CHAPTER VI

C-PROBE CALIBRATION

A. Adjusting the Probe Sensitivity

The sensitivity of the probe is determined by both the phase difference between the antenna and reference signals as well as the magnitudes of the two signals. For the phase discriminator utilized in this design, the greatest resolving power occurs when the reference signal and antenna signal start 90° apart from each other. This is the point where the slope of the DC output value per degree phase change is the greatest. Since we were trying to resolve both the real and imaginary parts of the signal, we required two signals 90° apart from each other. This means that either the real or imaginary parts of the measurement has better signal to noise resolution. Since the purpose of implementing a super-heterodyne system is to measure the small real component of the antenna impedance more accurately, it is the real component that was offset by 90° from the reference signal during calibration.

Two adjustments can be made to maximize the resolution between reactive and resistive components of impedance. The first is to ensure that the input levels into the phase discriminator's multiplier are close to the maximum allowed input. The second is to preset the phase difference between the reference signal and the intermediate signal. Since the DC output signal is directly related to the magnitude of the two signals being multiplied, the larger these two signals are, the larger the output swing will be and hence the better the resolution. The phase difference between the reference signal and the antenna signal can be adjusted by presetting a delay for the reference signal in the Altera. This is accomplished by passing the reference signal through a series of logic gates, which each have a slight delay, thus producing an effective phase shift

The problem of random start-up states for the Altera had its biggest affect on the ability to adjust the resolution. Since the resolution is partially dependent on the relative phases between the reference signal and intermediate signal at start-up, the inability to control the Altera's start-up states meant the inability to control the resolution. Even though the real and imaginary reference outputs from the Altera were 90° apart, the relative phase difference from these two and the intermediate signal could take on one of 32 different phases. This caused two major problems with the probe. First, the free-space capacitance could not be canceled out with the RF Head tuning capacitor. This process is done when the payload is still in the lab and can be adjusted by hand. When it is out on the launch pad, the relative difference between the reference signal and intermediate signal must be the same as it was in the lab to ensure the tuning capacitor is properly cancelling out the free-space capacitance. Another problem is that of saturating the output of the phase discriminator. If the relative phase differences could be controlled, the total amount of phase change would range at most 110° out of 360°. This includes the 90° of separation between the real and imaginary components as well as the 20° of maximum change expected from the plasma itself. In order to compensate, the gain on the discriminator must be reduced so that all 32 states can be accommodated.

B. Calibration Charts

The calibration of the C-probe was done using both a series of capacitors and resistors. Each calibrator was attached to the antenna and then to the signal ground of the C-probe. This configuration simulates the antenna in either a purely resistive or capacative medium. Unfortunately, because of the random start-up state problem induced by the Altera, we are unable to determine before calibration which output represents the real or imaginary component. The method I used to determine the outputs was to test the full range of capacative and resistive values. Whichever channel had the largest swing when the capacitors were placed on the

antenna, that was the imaginary channel. The same process was used to determine the real component. Table III through X shows the calibrations made with the capacitors and resistors.

TABLE III
CAPACITANCE CALIBRATION 1

Capacitance Calibration (pf)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
2.0	-2.15	1.25
3.0	-2.25	1.36
6.0	-2.21	1.62
6.25	-2.2	1.7
6.5	-2.16	1.7
6.75	-2.14	1.75
7.0	-2.15	1.7
7.25	-2.1	1.75
7.5	-2.12	1.75
7.75	-2.11	1.79
8.0	-2.15	1.82
15.0	-2.07	2.32
24.0	-2.07	2.85

TABLE IV
RESISTANCE CALIBRATION 1

Calibration Resistance (kΩ)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
1	-5.0	2.1
5	--3.0	1.45
10	-2.66	1.3
50	-2.38	1.2
100	-2.3	1.21
2200	-2.25	1.25

TABLE V
CAPACITANCE CALIBRATION 2

Capacitance Calibration (pf)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
2.0	-2.8	.55
3.0	-2.7	.7
6.0	-2.32	.96
6.25	-2.3	1.0
7.0	-2.2	1.1
8.0	-2.12	1.18
15.0	-1.53	1.9
24.0	-1.1	2.7

TABLE VI
RESISTANCE CALIBRATION 2

Calibration Resistance (kΩ)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
1	-5.0	4.7
5	-3.86	1.34
10	-3.24	.92
50	-2.98	.55
100	-2.95	.51
2200	-2.9	.43

TABLE VII
CAPACITANCE CALIBRATION 3

Capacitance Calibration (pf)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
2.0	-.89	1.08
3.0	-2.99	2.0
6.0	-2.72	1.9
7.0	-2.61	1.85
8.0	-2.5	1.85
15.0	-1.62	1.43
24.0	-.84	.97

TABLE VIII
RESISTANCE CALIBRATION 3

Calibration Resistance (kΩ)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
1	-.10	5.0
5	-2.6	3.38
10	-2.99	2.85
50	-3.37	2.45
100	-3.35	2.4
2200	-3.3	2.2

TABLE IX
CAPACITANCE CALIBRATION 4

Capacitance Calibration (pf)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
2.0	-1.02	.65
3.0	-1.2	.87
6.0	-1.4	1.17
7.0	-1.52	1.26
8.0	-1.61	1.38
15.0	-2.16	2.08
24.0	-2.7	2.68

TABLE X
RESISTANCE CALIBRATION 4

Calibration Resistance (kΩ)	Capacitance Channel Output (volts)	Conductance Channel Output (volts)
1	-5.0	-1.4
5	-2.15	-.10
10	-1.57	.20
50	-1.21	.50
100	-1.01	.50
2200	-1.02	.57

By observing the series of four calibration charts, it is apparent that the resolution range is different for each test. This is based on the relative phase difference between the intermediate signal and reference signal at start-up. As stated in the previous section, the start-up state could

not be predicted. The relative phase difference can fall within 32 states, which can range anywhere from 0 to 360°. The real and imaginary channels are also dependent on the relative phases and can randomly switch between start-up states. What this means is that the only way to determine which output represents the real or imaginary states is by evaluating the flight data during or after launch. Although these calibrations do not provide all possibilities, they do show that the resolution changes based on the start-up states of the Altera.

C. Performance Through Environmental Testing

The performance of the C-probe during environmental testing can only be evaluated through the telemetry provided by the entity conducting the environmental testing. Since the C-probe's power is cycled numerous times during the environmental testing, I am able to observe the power-up states of the Altera through the DC output of the phase discriminator as the output is presented in the telemetry. Through all environmental testing, the DC output never exceeded 2 volts.

CHAPTER VII

CONCLUSION AND RECOMMENDATIONS

A. Conclusion

Through the course of this project, I created a super-heterodyne C-probe that had the capability of improving the sensitivity of current C-probe designs. Unfortunately it was unreliable and would not be practical to implement on future spacecraft without fixing some of the observed problems. The design, construction, and testing process started by making observations as to how previous C-probes measured the impedance of an antenna in a plasma and how integrating the super-heterodyne technique into the old design would increase the sensitivity of the probes to a level where the real component of the antenna impedance could be measured. The next phase was to design the super-heterodyne system and integrate it into the existing C-probe design. Implementing the super-heterodyne technique required components that were capable of handling frequencies up to 400 MHz. Most of these high-frequency components were obtained as by-products from the cellular phone industry and were ideal for the frequencies and precision needed for this project. Although the super-heterodyne technique has been around since before the birth of impedance probes, it has only been recently practical to implement because the demand for cellular technology has only recently provided for the mass production of these components.

The predicted optimal operating condition of the construction and testing phase was overshadowed by the failure of the probe to start up in the same state each time. The ability to tune out the free-space capacitance of the antenna attached to the probe is based on the premise that the start-up conditions on the probe will be identical each time it is turned on. The programmable logic chip I chose to use had 32 separate start-up conditions and made the process of tuning the RF Head almost impossible. The result was a significant decrease in the sensitivity

of the probe and the inability to determine which channel was the capacitance channel and which was the conductance channel.

The theory of integrating a super-heterodyne system with the current C-probe design was proven by the simple fact that when the calibrations were done, there was a separate response between the two measured channels. Although the response could not be controlled or predicted, it did provide enough sensitivity based on the calibration curves to warrant it to be mounted to a sounding rocket for testing. Unfortunately, the rocket failed to reach altitude and the instrument was never tested as a flight system.

My experience with the flight operations of the probe was invaluable in understanding the changes in RF noise between the rocket and lab bench. The ability to shield the instrument is crucial. The independent power source is a critical factor in the design. My DC-to-DC converters were the cause of most of the high-frequency problems inside the probe's protective casing. The extreme environmental testing was an indication of just how severe the mechanical stresses are. This caused me to take such precautions as gluing all the components to the board.

B. Recommendations for Further Research

First and foremost, my biggest recommendation would be to investigate why the Altera never started up in-phase with the intermediate signal. If this phasing problem is not solved, the super-heterodyne C-probe would be no different in performance than the previous probes and depending on the state it randomly starts up in, the super-heterodyne C-probe could be worse than previous probes in terms of probe sensitivity. I would recommend finding a way to force the start-up conditions to always be the same to ensure that the relative phases of the reference and current signals are constant for all start-ups.

The next recommendation for further research would be with the RF Head. The ideal configuration for this device has always been contested. This component is the heart of the

impedance probe and will continue to be so as long as we continue measuring the current signal from the antenna. Along with the design of the RF Head, I would recommend research into the signals driving the RF Head. Currently, I am using a square wave, which still contains the fundamental frequency but requires that some filtering be done after the RF Head. I would recommend that if the space exists, a filter should be added before the RF Head. The phase shift induced will be the same, but the requirements for filtering and gain will be much less on the RF Head post-amp.

The next recommendation I have would be to increase the intermediate frequency. The current design has the intermediate frequency at around 23 KHz. I found this to be rather close to the sample rate required for the A/D converters and found that the anti-aliasing filter had a cutoff frequency that was too high for the phase discriminator filter. Since these two filters are implemented with the same active filter, I found that I was left with some ripple in the DC output of the phase discriminators. By increasing the intermediate frequency, you decrease the source frequency and division ratios can be decreased. This means cheaper parts, less high-frequency noise, and easier filtering. I would recommend moving the intermediate frequency to 50 KHz.

Another recommendation I have is to eliminate the RF filter and perform all the filtering with the intermediate filter [8]. By designing the intermediate filter as a double-tuned filter, the phase shift induced by that filter will be 0. This design is also less susceptible to temperature variations, making it ideal for spaceflight.

The recommendations I have made have all been intended to increase the sensitivity of the probe. The first deals with solving a problem that is inherent in the logic I chose to use. Either the problem with the Altera must be solved, or another programmable logic chip must be used. The second recommendation is valid for all probes using the RF Head and is not as imperative as the first recommendation. The last recommendation is not critical and may not

significantly help with sensitivity, but it will greatly simplify the construction phase and may help to lower the cost for future super-heterodyne C-probes.

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[7] C. Swenson. 6 May, 1997, Private Communication.

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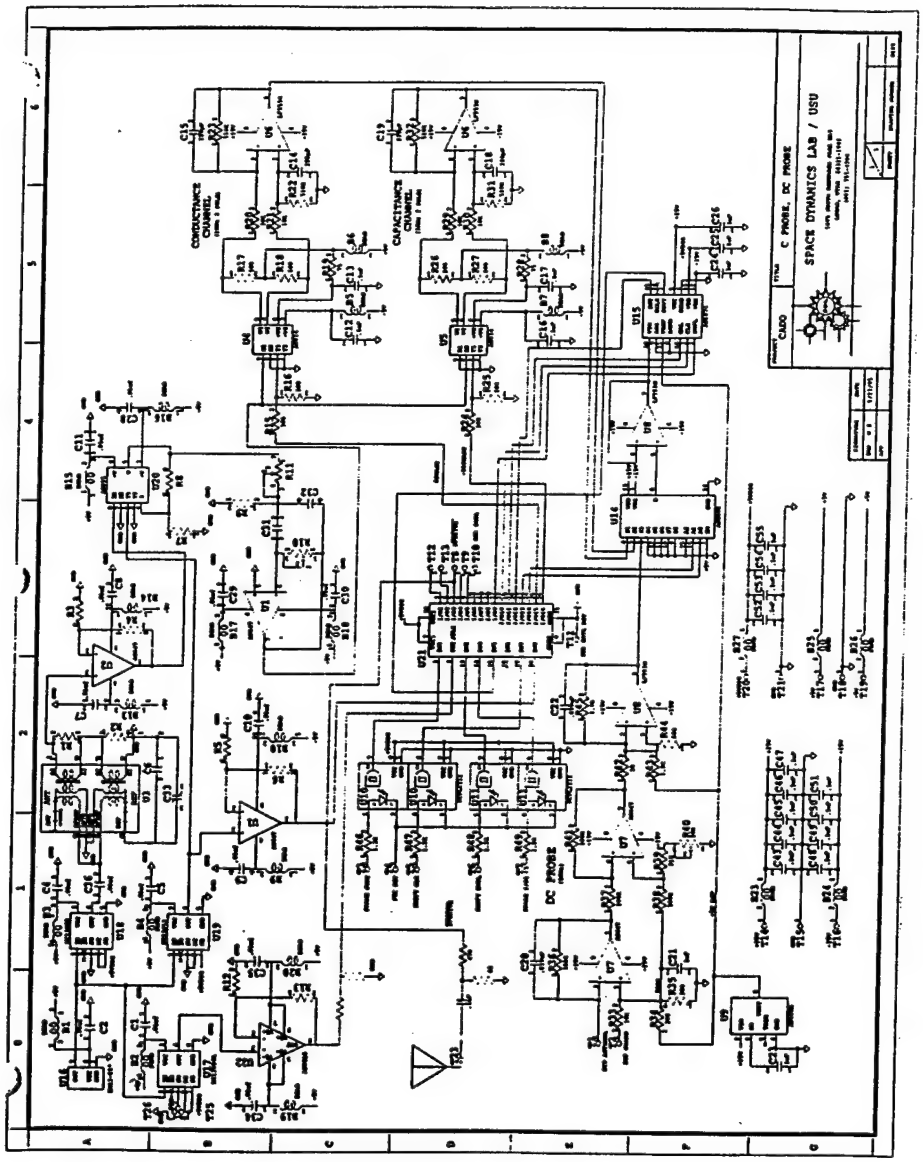
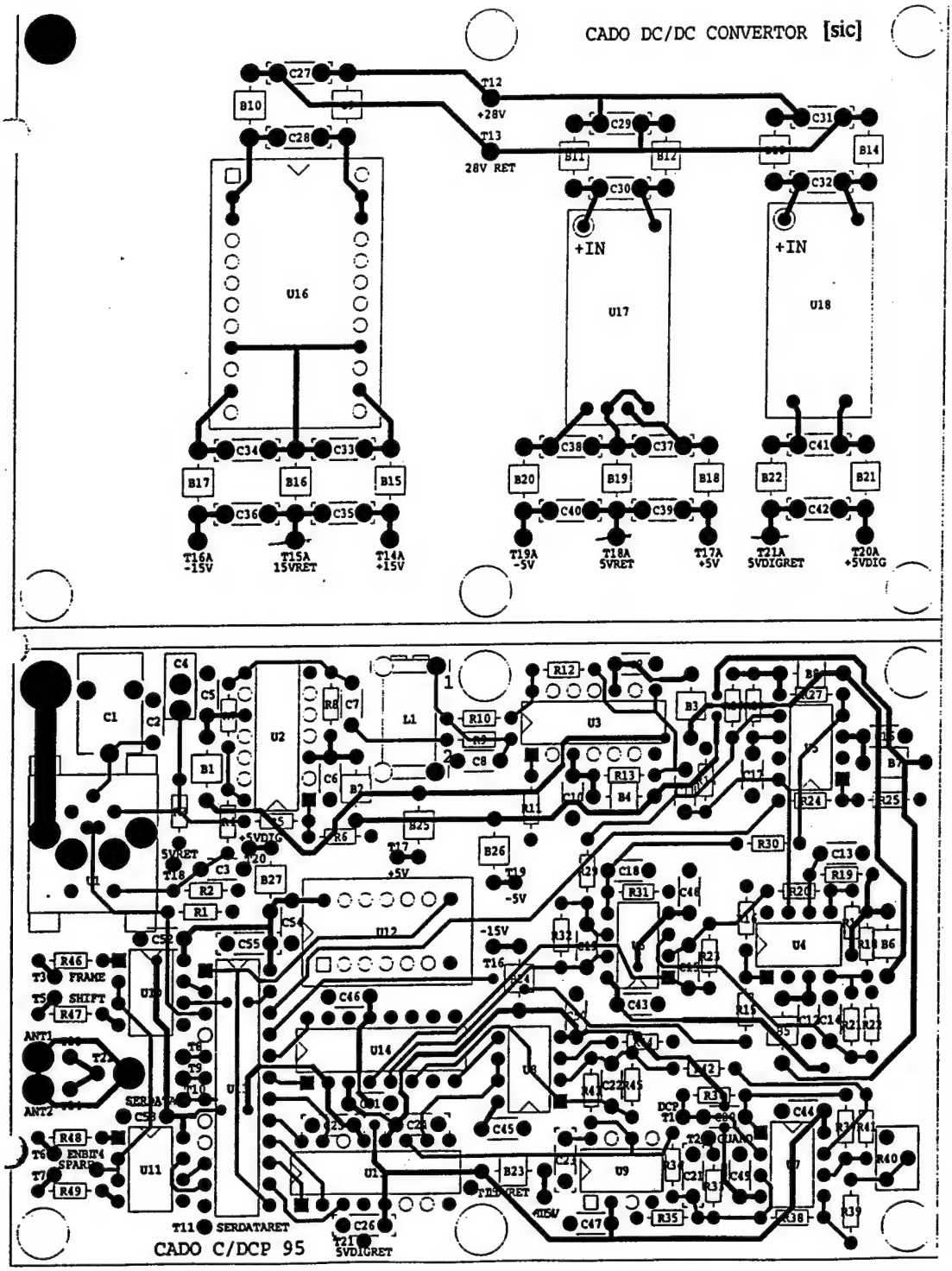
APPENDICES

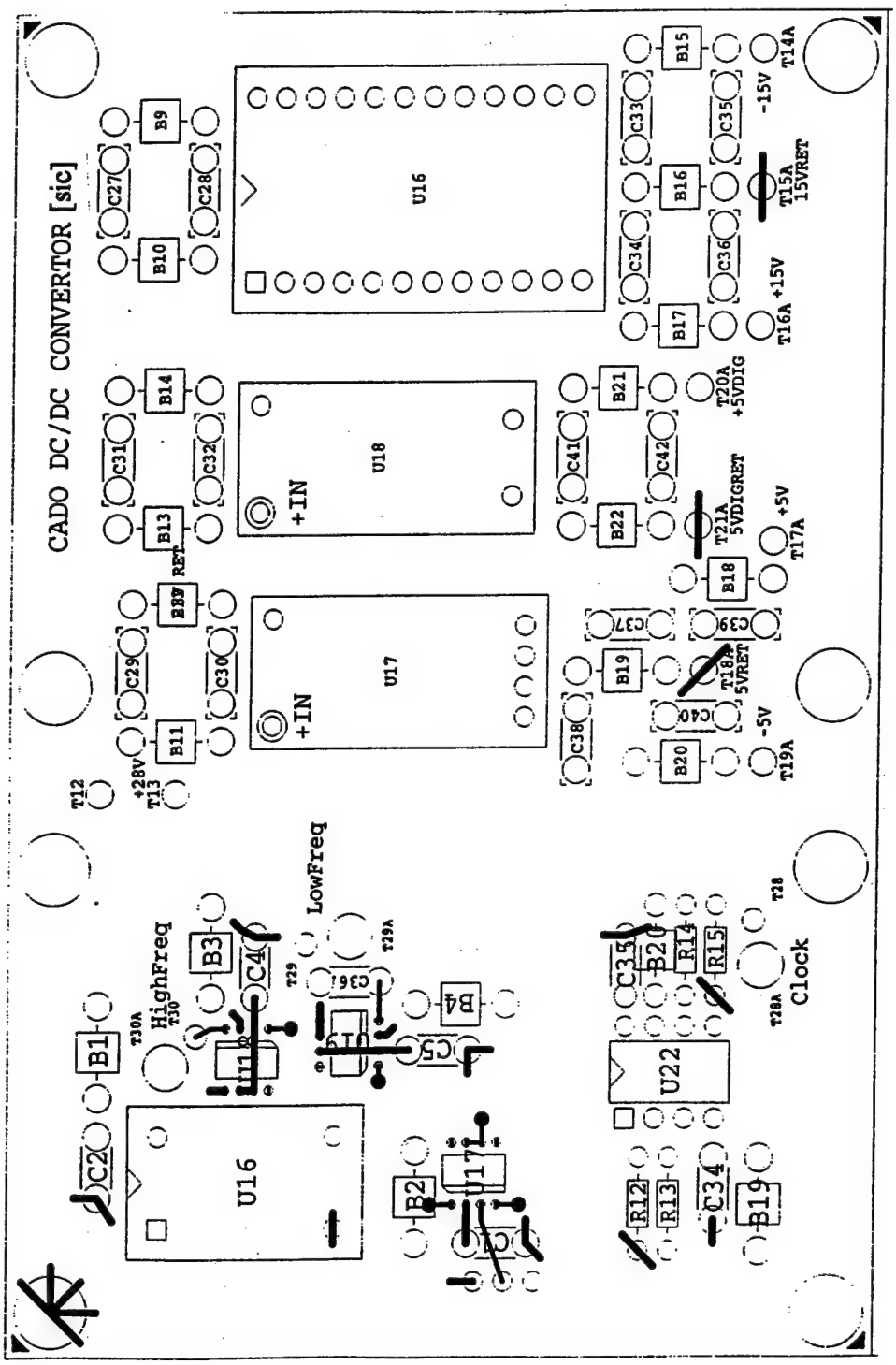
Appendix A. Schematic Diagram


SPACE DYNAMICS LAB / USU
C PROBE, DC PROBE
CONDUCTANCE CHANNEL
CAPACITANCE CHANNEL
DC PROBE

Appendix B. CADO Capacitance Probe Trace Layout


CADO DC/DC CONVERTOR [sic]
C27
T12
+28V
T13
28V RET
B10
C28
C29
C31
B11
B12
B14
C30
C32
+IN
+IN
U16
U17
U18
C34
C33
B17
B16
B15
C36
C35
T16A
-15V
T15A
15VRET
T14A
+15V
C38
C37
B20
B19
B18
C40
C39
T19A
-5V
T18A
5VRET
T17A
+5V
C41
B22
B21
C42
T21A
5VDIGRET
T20A
+5VDIG
CADO C/DCP 95

Appendix C. Circuit Ground Trace Layout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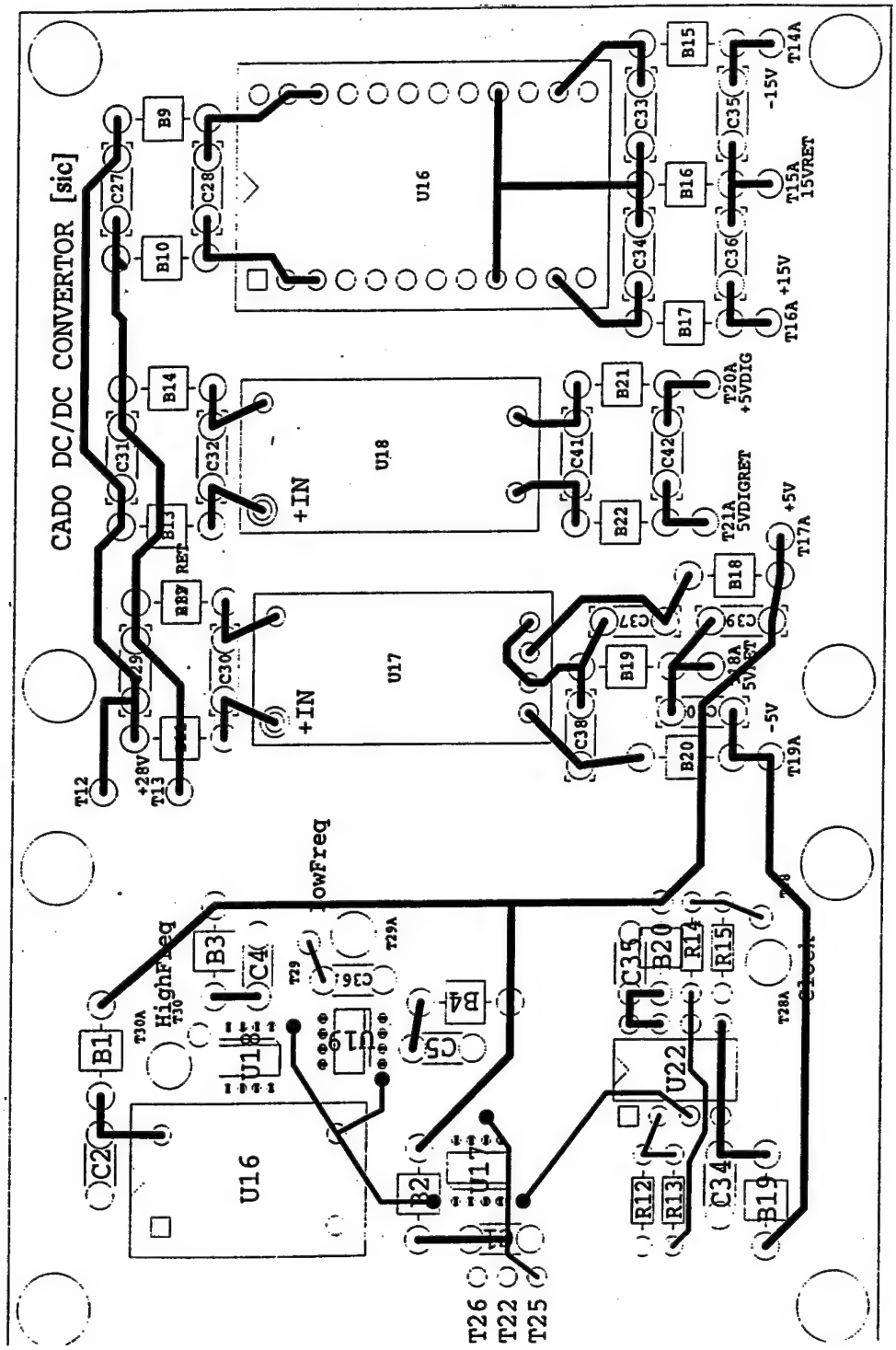
U18
U17
U22
+IN
HighFreq
LowFreq
Clock
+28V
RET
+5V
-5V
+15V
-15V
5VDIGRET
5VRET
15VRET


CADO DC/DC CONVERTOR [sic]
U16
U18
U17
U22
+IN
+IN
T12
T13
+28V
T14A
-15V
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15VRET
T16A
+15V
T17A
+5V
T19A
-5V
T20A
+5VDIG
T21A
5VDIGRET
T22
T25
T26
B1
B2
B3
B4
B9
B10
B14
B15
B16
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B21
B22
C2
C4
C5
C27
C28
C30
C31
C32
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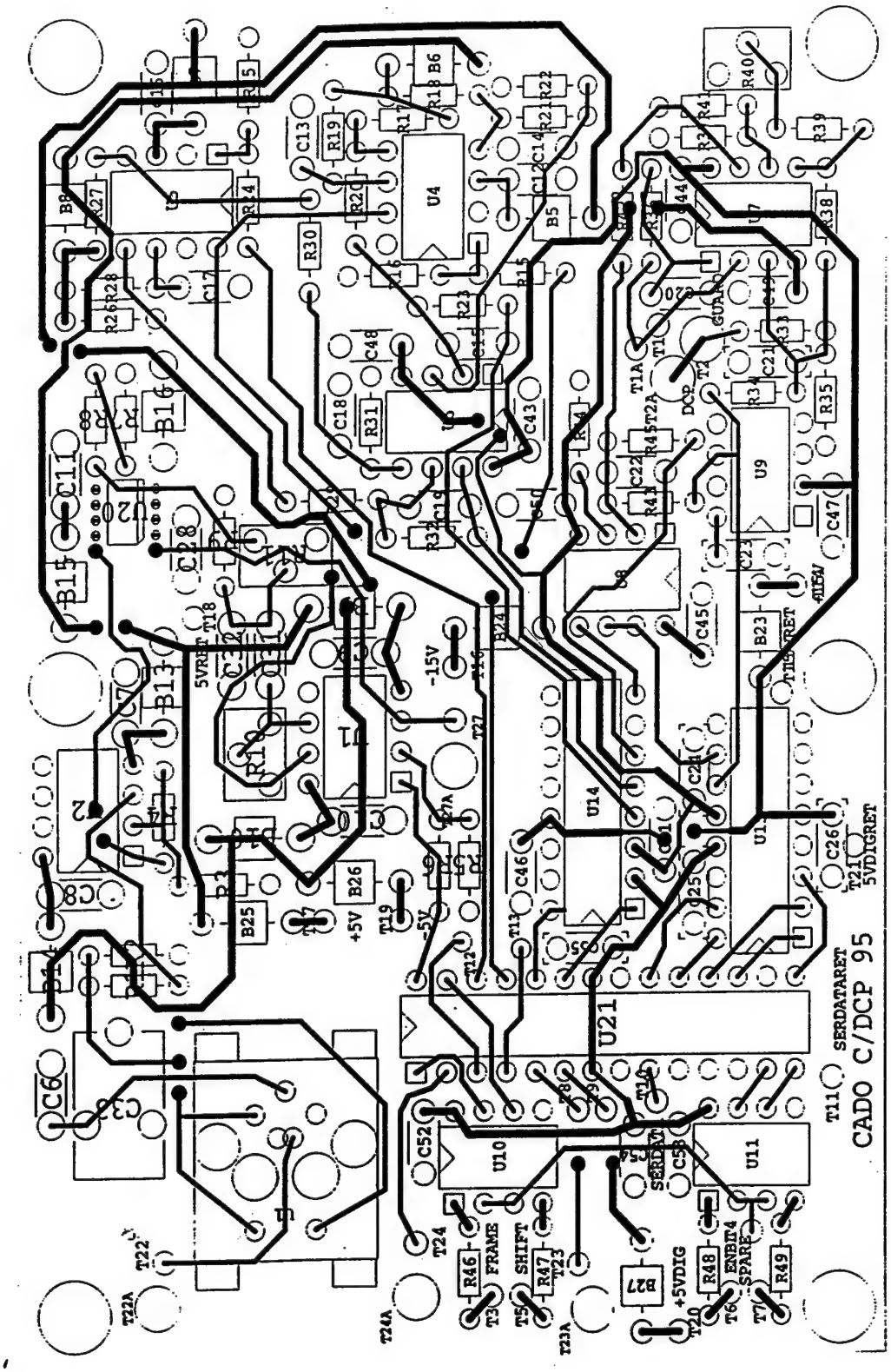
C39
C41
C42
R12
R13
R14
R15

Appendix D. Signal and Power Circuit Trace Layout


CADO C/DCP 95
SERDATARET
5VDIGRET
U21
U14
U10
U11
U9
U4
SERDATA
FRAME
SHIFT
SPARE
ENBDT4
+5VDIG
+5V
-5V
-15V
5VREF
T11
T12
T13
T14
T15
T16
T17
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T21
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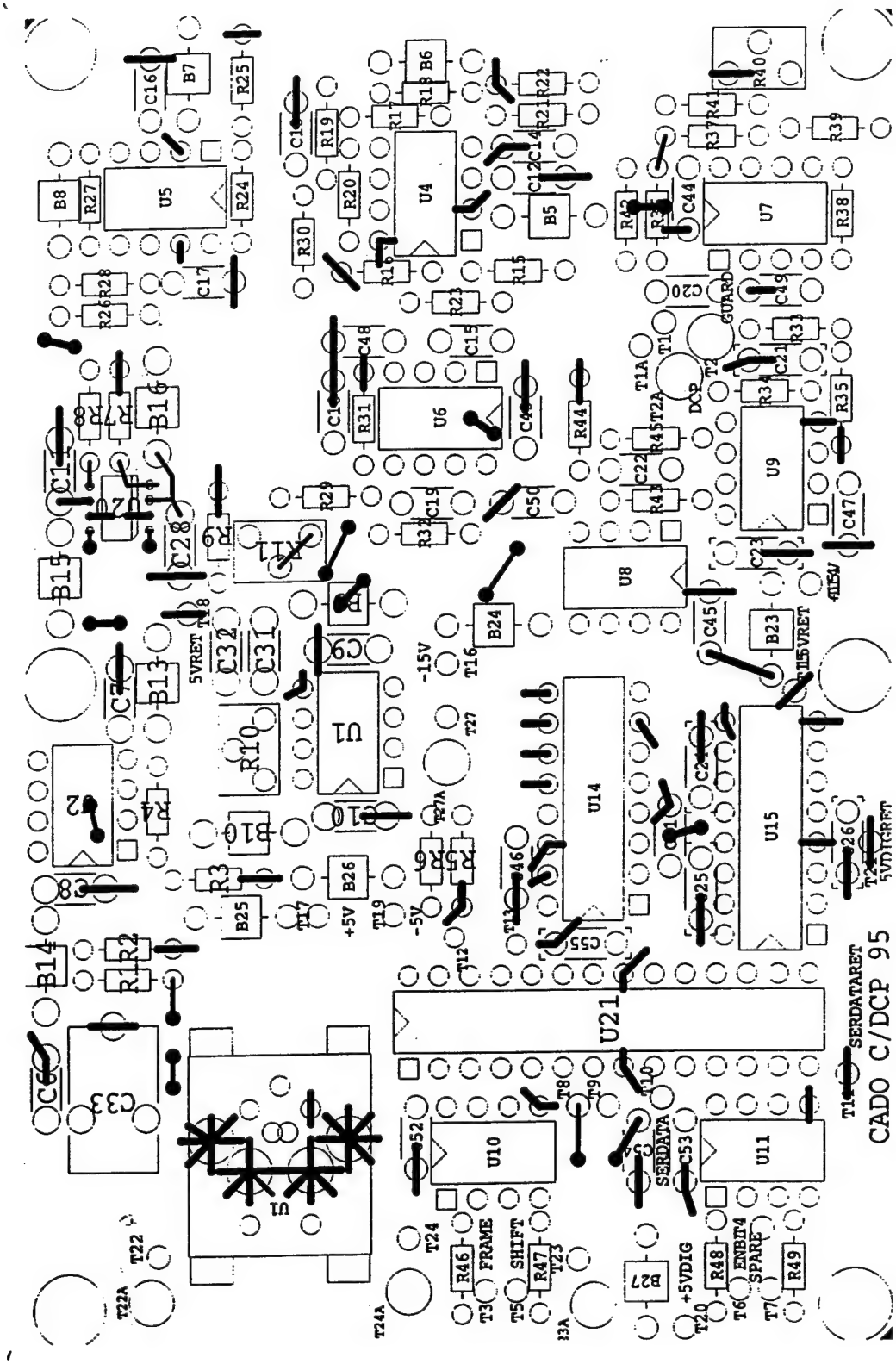
T24
T1A
T2A
T22A
T23A
T24A


CADO C/DCP 95
U21
U14
U15
U10
U11
U1
U2
U4
U5
U6
U7
U8
U9
SERDATA
SERDATARET
FRAME
SHIFT
SPARE
ENBD4
+5VDIG
+5V
-5V
-15V
5VRET
GUARD

Appendix E. Altera Code

```
%****************************
*                           *
* COORS--DC_C PROBE Digital *
*                           *
*   SCOTT HERITSCH          *
*                           *
*   July 08, 1997           *
*                           *
****************************%
SUBDESIGN    DC_C_Dig

(
        XTAL, MFS, ENABLE, S_CLK, DOUT, BSY, INVSEC          :INPUT;

        SMPL, ADCLK, CAL, SER_DATA, MUXA0, MUXA1,
        P_0, P_90, P_180, P_270, RF_DNOT,SEC                 :OUTPUT;
)

VARIABLE

        MUXA0, MUXA1                                         :JKFF;
        CAL_CLK, MSB, N_CLK, INT, CLK                        :NODE;

        CONT            :MACHINE OF BITS (B[3..0])
                                WITH STATES (       C1 = 0,
                                                    C2 = 1,
                                                    C3 = 2,
                                                    C4 = 3,
                                                    C5 = 4,
                                                    C6 = 5,
                                                    C7 = 6,
                                                    C8 = 7,
                                                    C9 = 8,
                                                    C10 = 9,
                                                    C11 = 10,
                                                    C12 = 11,
                                                    C13 = 12,
                                                    C14 = 13,
                                                    C15 = 14,
                                                    C16 = 15 );

        INTDIV[4..0]                                         :DFF;

        DIV1            :MACHINE OF BITS (Q[1..0])
                         WITH STATES ( D1 = 0,
                                       D2 = 1,
                                       D3 = 2,
                                       D4 = 3 );

        RFNOT           :MACHINE OF BITS (F[1..0])
                        WITH STATES (G1 = 0,
```

```
                                                    G2 = 1,
                                                    G3 = 2,
                                                    G4 = 3 );

BEGIN

        CLK = XTAL;
        MUXA0.CLK = CLK;
        MUXA1.CLK = CLK;
        SEC = !INVSEC;


        ADCLK = (!CAL_CLK AND S_CLK AND !N_CLK)
                OR (CAL_CLK AND ENABLE);


        IF MSB THEN
                SER_DATA = !DOUT;
        ELSE
                SER_DATA = DOUT;
        END IF;


        INTDIV[].CLK = SEC;

        INTDIV[].d = INTDIV[].q+1;

        INT = INTDIV[4];


        DIV1.CLK = INT;

        CASE DIV1 IS

                WHEN D1 =>
                        P_90 = VCC;
                        P_180 = VCC;
                        DIV1 = D2;

                WHEN D2 =>
                        P_90 = VCC;
                        P_0 = VCC;
                        DIV1 = D4;

                WHEN D3 =>
                        DIV1 = D1;
                        P_180 = VCC;
                        p_270 = VCC;

                WHEN D4 =>
                        P_0 = VCC;
```

```
                P_270 = VCC;
                DIV1 = D3;

END CASE;


RFNOT.CLK = CLK;

CASE RFNOT IS

        WHEN G1 =>
                RFNOT = G2;

        WHEN G2 =>
                RFNOT = G4;

        WHEN G3 =>
                RF_DNOT = VCC;
                RFNOT = G1;

        WHEN G4 =>
                RF_DNOT = VCC;
                RFNOT = G3;
END CASE;


CONT.CLK = SEC;

CASE CONT IS

        WHEN C1 =>
                IF MFS THEN
                        CONT = C2;
                ELSE
                        CONT = C1;
                END IF;

        WHEN C2 =>
                IF !MFS THEN
                        CONT = C4;
                ELSE
                        CONT = C2;
                END IF;

        WHEN C3 =>
                CAL_CLK = VCC;
                IF !BSY THEN
                        CONT = C7;
                ELSE
                        CONT = C3;
                END IF;

        WHEN C4 =>
                CAL = VCC;
```

```
        CAL_CLK = VCC;
        IF MFS THEN
                CONT = C3;
        ELSE
                CONT = C4;
        END IF;

WHEN C5 =>
        N_CLK = VCC;
        CONT = C6;

WHEN C6 =>
        CONT = C14;

WHEN C7 =>
        SMPL = VCC;
        N_CLK = VCC;
        IF S_CLK THEN
                CONT = C5;
        ELSIF MFS THEN
                CONT = C8;
        ELSE
                CONT = C7;
        END IF;

WHEN C8 =>
        MUXA0.K = VCC;
        MUXA1.J = VCC;
        IF !ENABLE AND !MFS THEN
                CONT = C7;
        ELSE
                CONT = C8;
        END IF;

WHEN C9 =>
        MSB = VCC;
        IF S_CLK THEN
                CONT = C10;
        ELSE
                CONT = C9;
        END IF;

WHEN C10 =>
        IF !BSY THEN
                CONT = C12;
        ELSE
                CONT = C10;
        END IF;

WHEN C11 =>
        MUXA1.K = VCC;
        IF !ENABLE AND !MFS THEN
                CONT = C7;
        ELSE
```

```
                    CONT = C11;
                END IF;

            WHEN C12 =>
                CONT = C16;

            WHEN C13 =>
                MSB = VCC;
                IF !S_CLK THEN
                    CONT = C9;
                ELSE
                    CONT = C13;
                END IF;

            WHEN C14 =>
                IF ENABLE THEN
                    MSB = VCC;
                    CONT = C13;
                ELSE
                    CONT = C14;
                END IF;

            WHEN C15 =>
                IF !ENABLE AND !MFS THEN
                    CONT = C7;
                ELSIF MUXA1 THEN
                    CONT = C11;
                ELSE
                    MUXA0.J = VCC;
                    CONT = C15;
                END IF;

            WHEN C16 =>
                IF !MUXA0 THEN
                    CONT = C15;
                ELSE
                    CONT = C8;
                END IF;

        END CASE;

END;
```